

TPV-INVENTA TECHNOLOGY CO., LTD. (TNI)

RDC2. EE Div. HW Department II

Board name : MotherBoard Schematic
Project : Nell (Nisene2 LarryBird)
Version : M0C
Initial Date : 2012/02/10
PCB P/N. : 6050A2516301
PCBA P/N. : 1310A2516301

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T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	M0B
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark	<remark>
Date	Tuesday, May 08, 2012	Sheet	1 of 43		

02 TABLE OF CONTENTS

CONTENTS	SHEET
01 TITLE PAGE	1
02 TABLE OF CONTENTS	2
03 SYSTEM BLOCK DIAGRAM	3
04 CLK/SMBUS/RESET MAP	4
05 CPU-CLK/CTRL/MISC/PEG (1/4)	5
06 CPU-Memory (2/4)	6
07 CPU-Power (3/4)	7
08 CPU-GND (4/4)	8
09 DDR3 SODIMM9.2 CHA	9
10 DDR3 SODIMM5.2 CHB	10
11 eDP to LVDS PS8625	11
12 MXM 3.0 TYPE-A	12
13 BACKLIGHT CTRL/CONVERTER	13
14 CP-PCI/E/DMI/USB/CLK (1/6)	14
15 CP-SATA/HOST/GPIO/VGA (2/6)	15
16 CP-SMB/LPC/AUDIO/RTC (3/6)	16
17 CP-POWER (4/6)	17
18 CP-GND/NVRAM/XDP (5/6)	18
19 CP STRAPS (6/6)	19
20 Audio Codec 92HD91/SSM2306	20
21 Audio DRV604/D-MIC	21
22 GIGA LAN RTL8171FH-CG/LED	22
23 CR/HDD/ODD/WEBCAM	23
24 MINI PCIe x 3/FAN	24
25 USB3.0 CONTROLLER	25
26 USB3.0/USB2.0 CONN	26
27 SCALAR/TOUCH SCREEN	27
28 EC IT8518E	28
29 DEBUG CIRCUIT	29
30 SYSTEM +3V/+5V	30
31 +1.5V_SUS/MEM_VTT/DC-IN	31
32 +1.05V/+1V	32
33 +0.85V/+12V	33
34 +1.8V/+1.1V/+19V_S0/DIS	34
35 NCP6133	35
36 NCP6133/MOS	36
37 POWER SEQUENCE	37
38 GPIO TABLE	38
39 HISTORY	39

XTAL LIST

	PARTS	DIP/SMT	Frequence	PPM	CL
1	X3	SMT	25MHz	±20	10pF/10pF
2	X4	SMT	25MHz	±20	10pF/10pF
3	X6	SMT	48MHz	±20	18pF/12pF
4	X5	SMT	32.768KHz	±20	7pF/7pF

USB LIST

PORT	NET NAME	FUNCTION
USB0N/P	USB0N/P	SIDE IO
USB1N/P	USB1N/P	SIDE IO
USB2N/P	USB2N/P	REAR IO
USB3N/P	USB3N/P	REAR IO
USB4N/P	USB4_WLAN_N/P	REAR IO
USB5N/P	USB5_TV_N/P	REAR IO
USB9N/P	USB9_DONGLE_N/P	WLAN CARD
USB10N/P	USB10_WEBCAM_N/P	TV CARD
USB11N/P	USB11_TSCREEN_N	DONGLE

PCIE LIST

PORT	NET NAME	FUNCTION
PETN/P2	PCIE_USB3_TXN/P	USB 3.0
PERN/P2	PCIE_USB3_RXN/P	
PETN/P3	PCIE_LAN_TXN/P	GIGA LAN
PERN/P3	PCIE_LAN_RXN/P	
PETN/P4	PCIE_CR_TXN/P	CARD READER
PERN/P4	PCIE_CR_RXN/P	
PETN/P5	PCIE_TV_TXN/P	TV CARD MODULE
PERN/P5	PCIE_TV_RXN/P	
PETN/P6	PCIE_WLAN_RXN/P	WLAN CARD MODULE
PERN/P6	PCIE_WLAN_TXN/P	

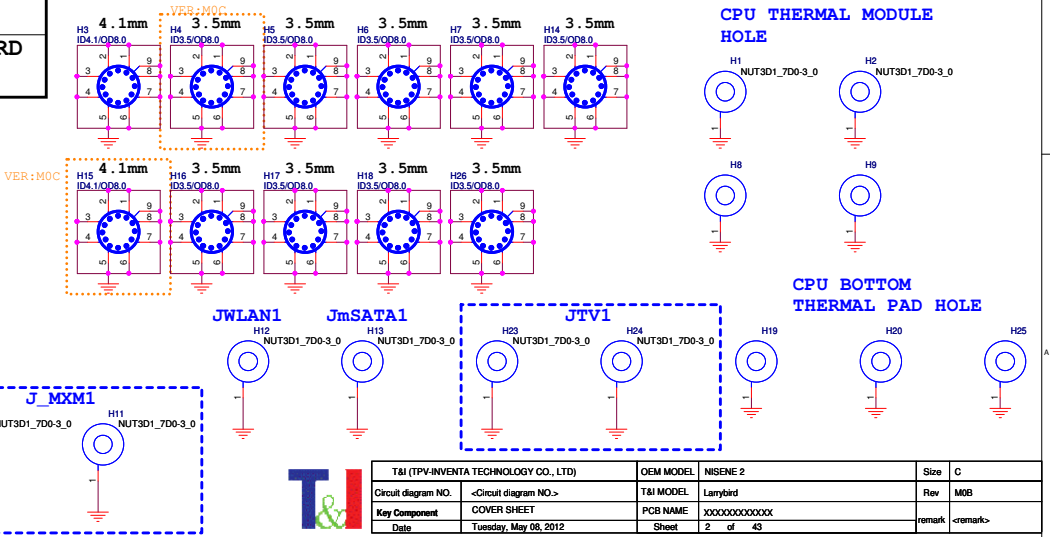
SATA LIST

PORT	NET NAME	FUNCTION
SATA0TXN/P	SATA_TX0N/P	SATA HDD
SATA0RXN/P	SATA_RX0N/P	
SATA1TXN/P	SATA_TX1N/P	mSATA
SATA1RXN/P	SATA_RX1N/P	
SATA4TXN/P	SATA_TX4N/P	SATA ODD
SATA4RXN/P	SATA_RX4N/P	

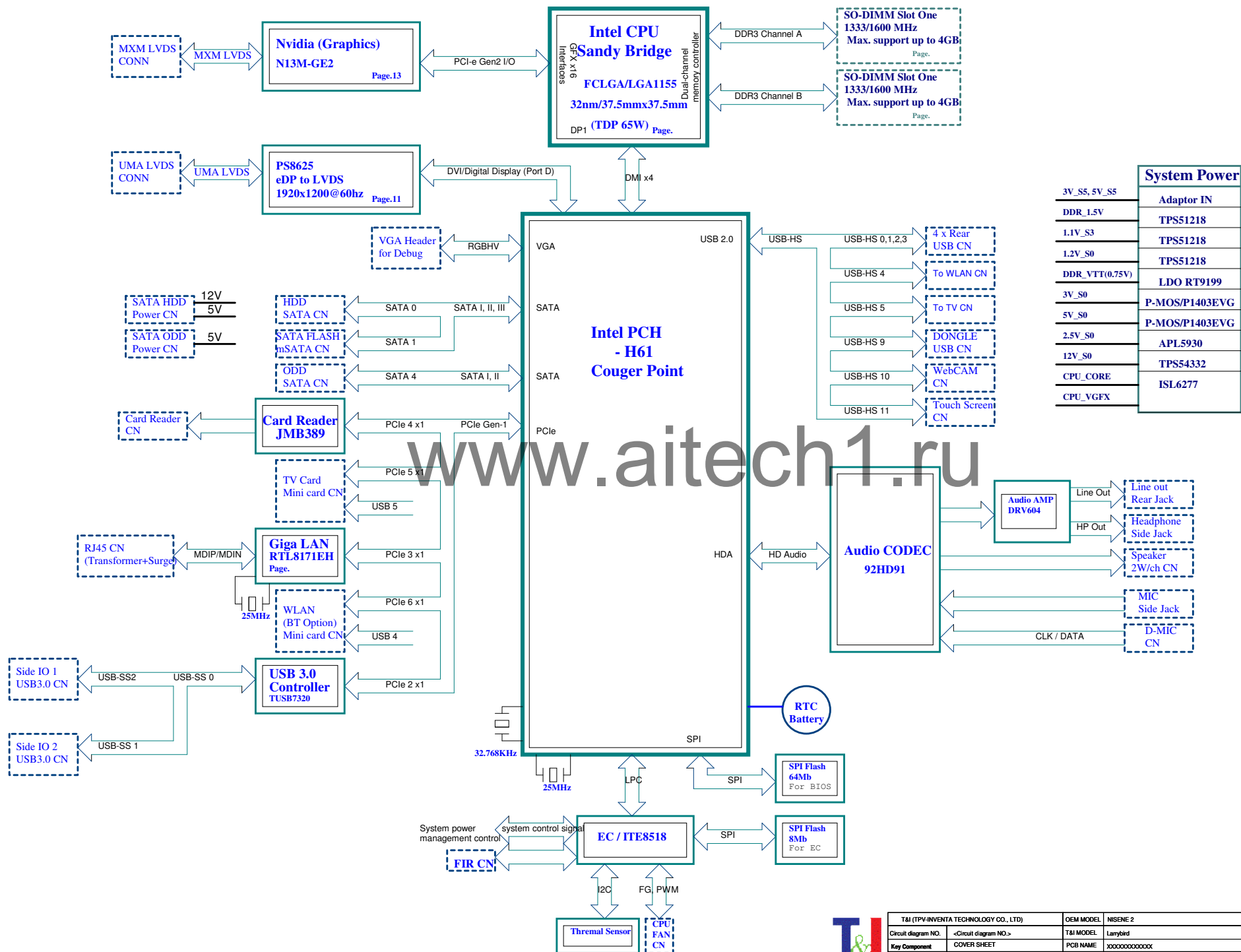
POWER STATES

STATE	SIGNAL	VOTAGE	S0	S3	S5	G3	REMARK
	FCH_SLP_S3#	-	HIGH	LOW	LOW	LOW	
	FCH_SLP_S5#	-	HIGH	HIGH	LOW	LOW	
	S5_PWR_ON	-	HIGH	HIGH	HIGH	LOW	S5_PWR_ON
ALWAYS	+VBAT_IN	+3.3V	0	0	0	0	COIN BATTERY
DC-in	+VIN	+19V	0	0	0	X	DC-IN
	+3V_LDO/+5V_LDO	+3.3V/+5V	0	0	0	X	
S5	+3V_S5	+3.3V	0	0	0	X	
	+5V_S5	+5V	0	0	0	X	
S3	+5V_S3	+5V	0	0	X	X	
	+3V_S3	+3.3V	0	0	X	X	
	+1.1V_S3	+1.1V	0	0	X	X	
	+1.5V_S3	+1.5V	0	0	X	X	
	+MEM_VTT	+0.75V	0	X	X	X	
	+3V_S0/+5V_S0	+3.3V/+5V	0	X	X	X	
	+12V_S0	+12V	0	X	X	X	
	+1.8V_S0	+1.8V	0	X	X	X	
	+1.5V_S0	+1.5V	0	X	X	X	
	+1.05V_S0	+1.05V	0	X	X	X	
	+CPU_VCCIO	+1.0V	0	X	X	X	
	+0.85V_S0	+0.85V	0	X	X	X	
	+CPU_AXG	SVC/SVD	0	X	X	X	
	+CPU_VCC	SVC/SVD	0	X	X	X	

ALWAYS
DC-in
S5
S3
S0



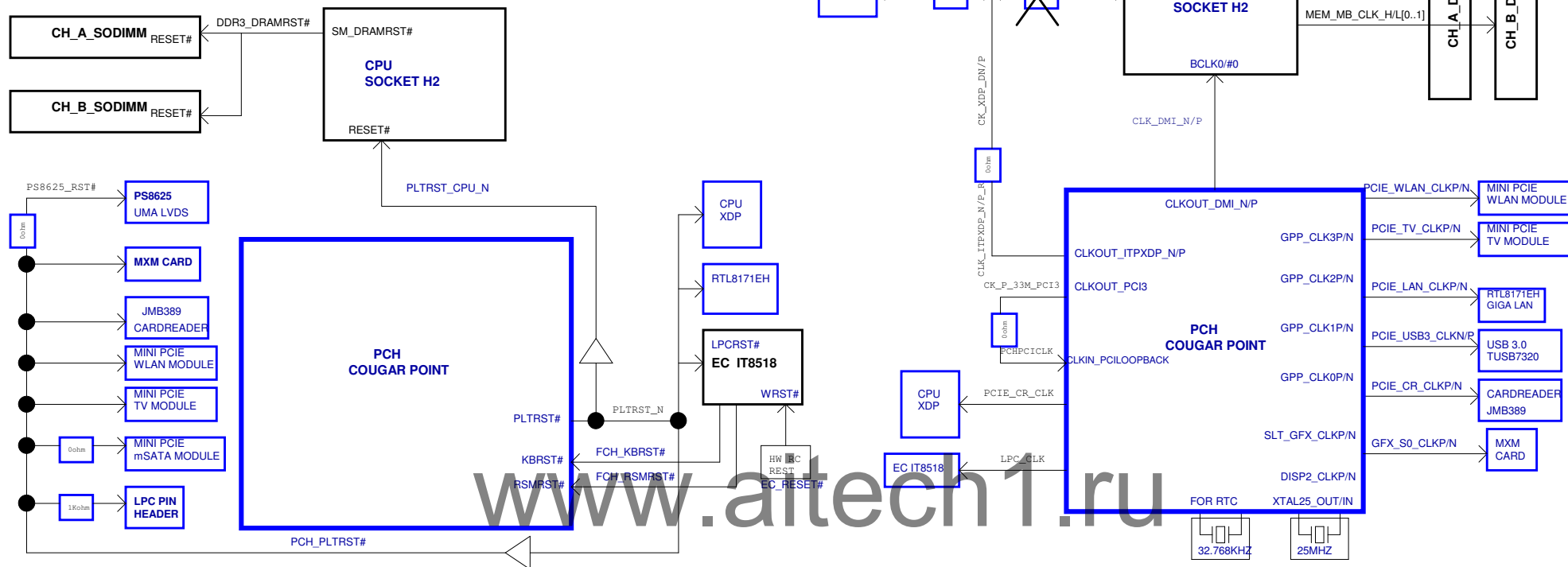
03 SYSTEM BLOCK DIAGRAM



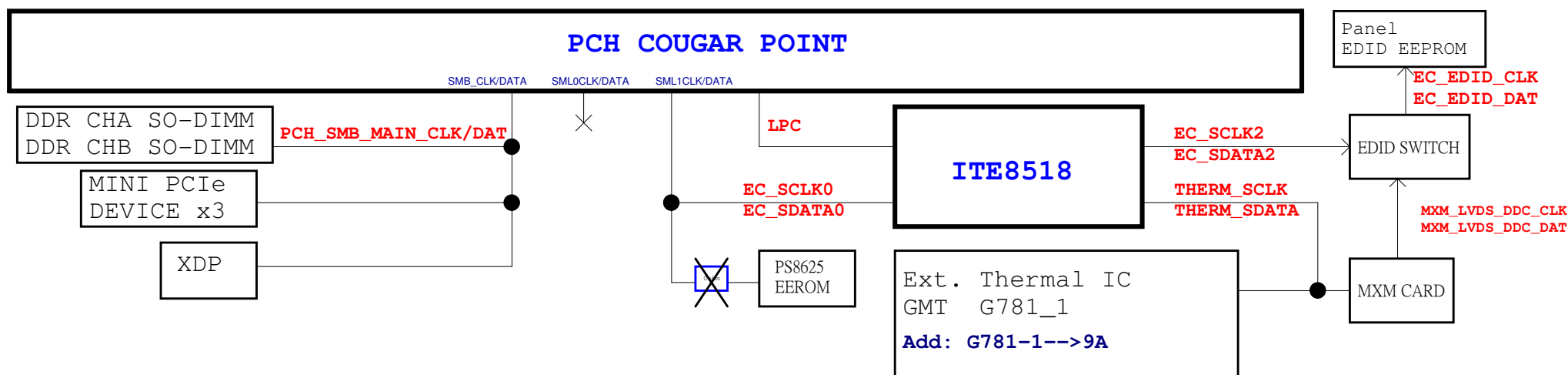
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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lamybird	Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXXXXXX	remark	<remark>
Date	Tuesday May 08, 2012	Sheet	3 of 43		

INTERNAL CLOCK MODE

RESET Block Diagram



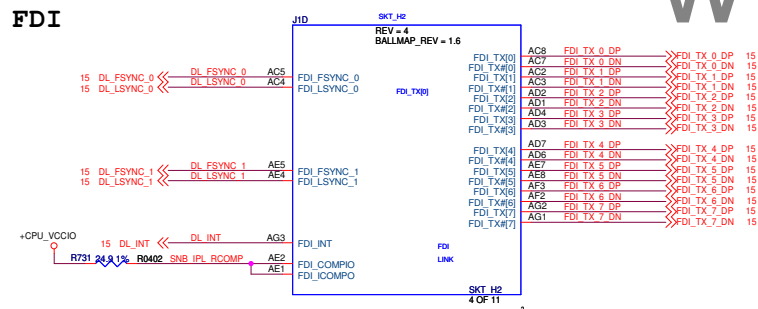
SM Bus MAP



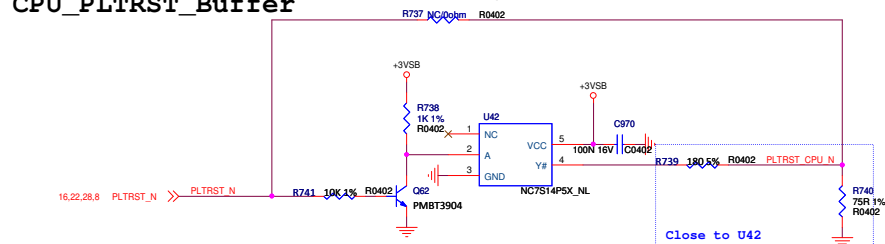
PCIEX16 & DMI



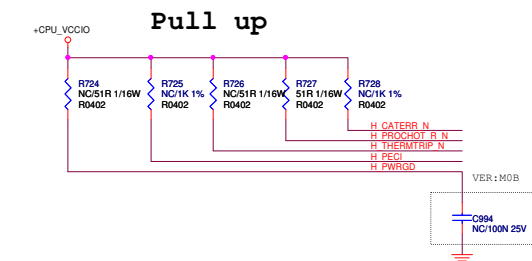
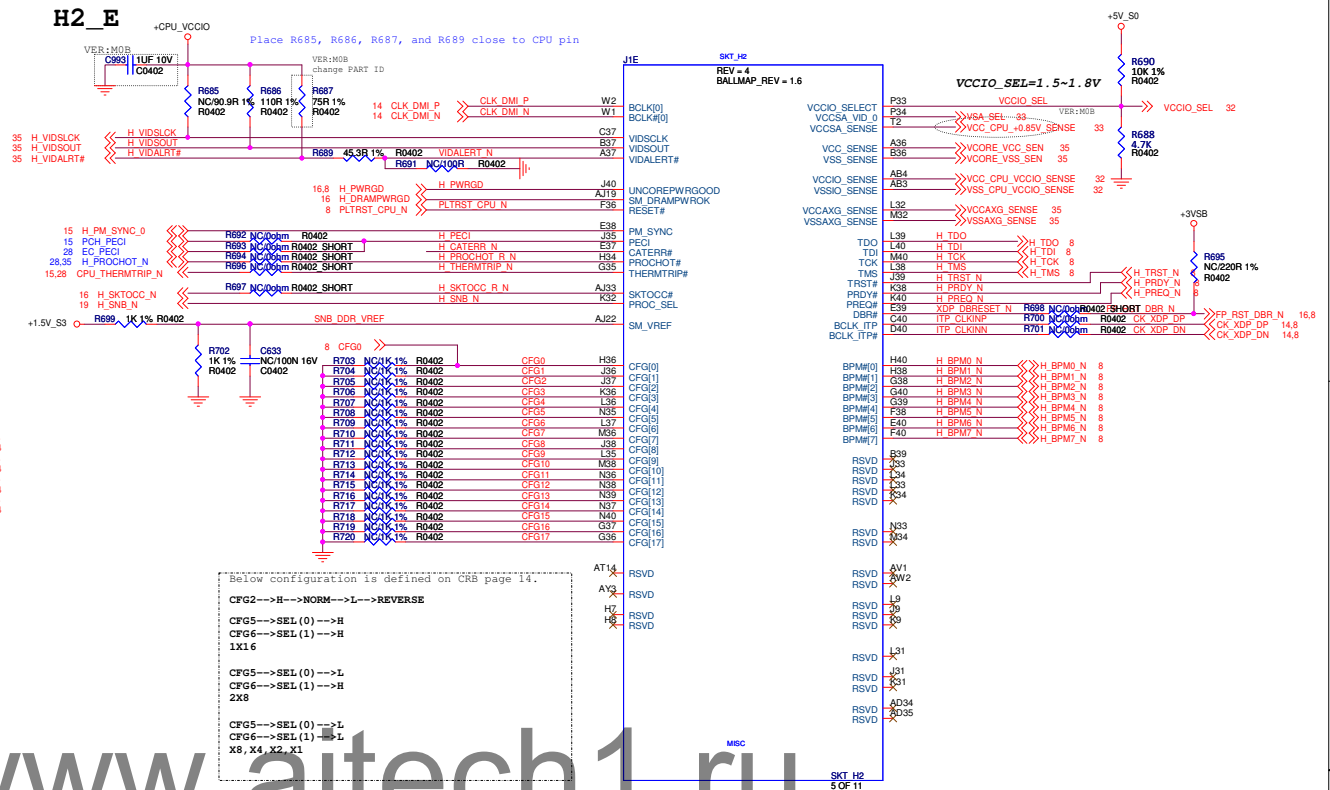
FDI

CPU_PLTRST_Buffer^I

CPU PLT_RST Buffer If PLT_RST driver current enough. need to use buffer

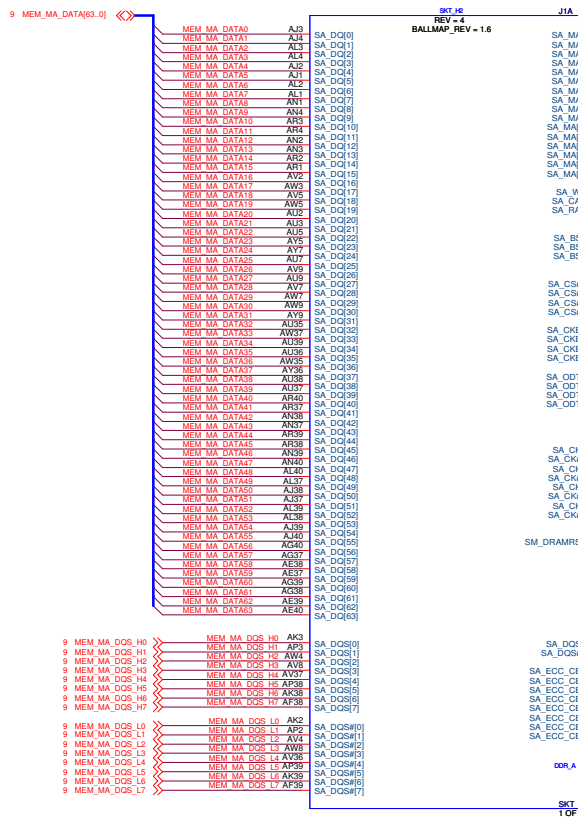


H2_E

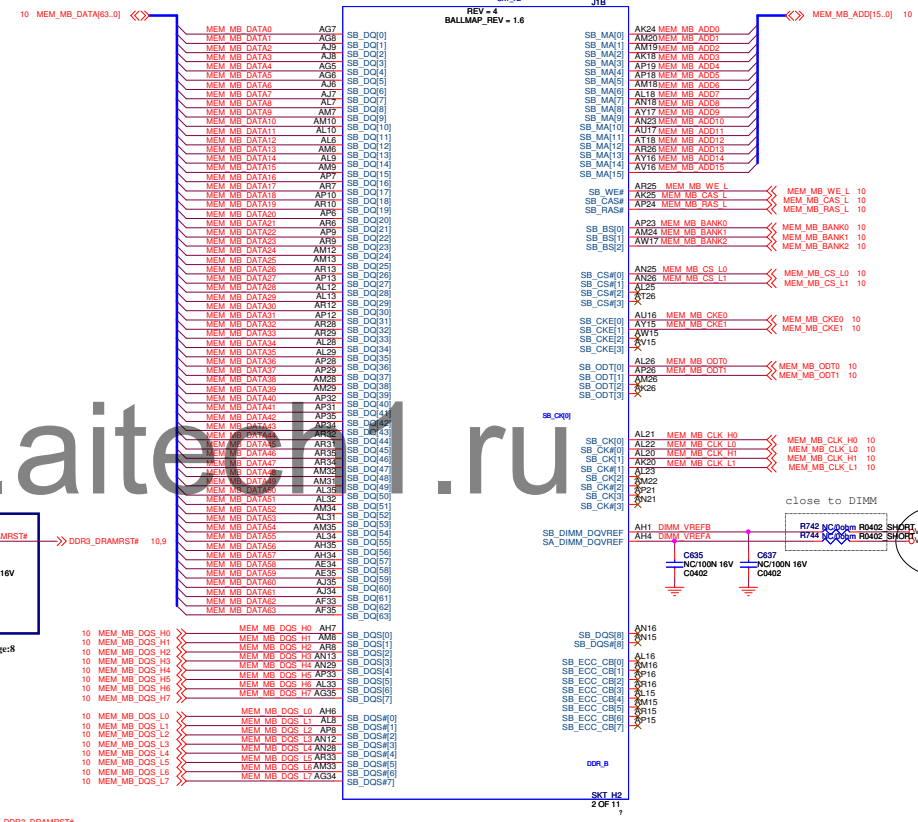


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Date	Tuesday, May 08, 2012	Sheet	5 of 43		

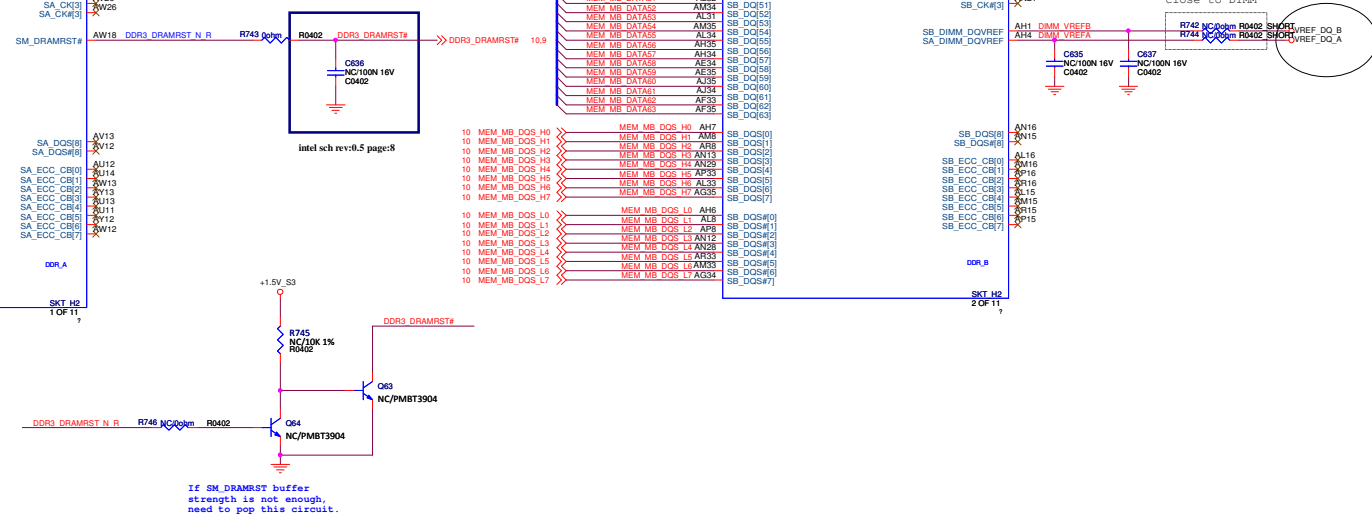
Channel_A



Channel_B

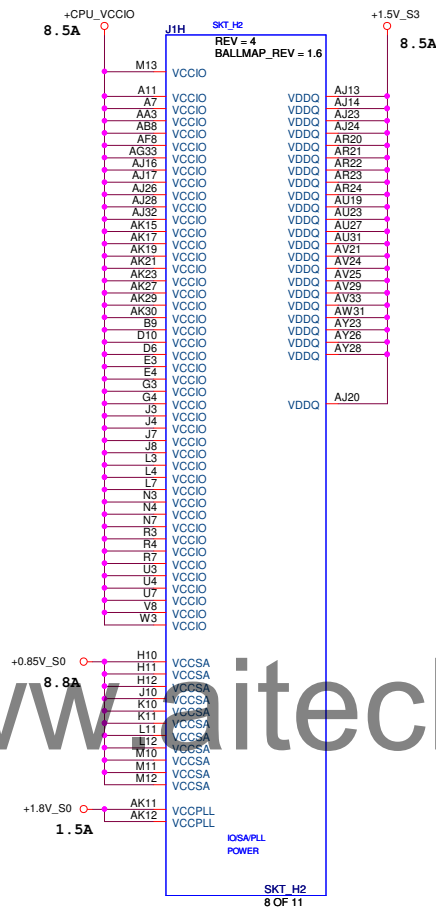
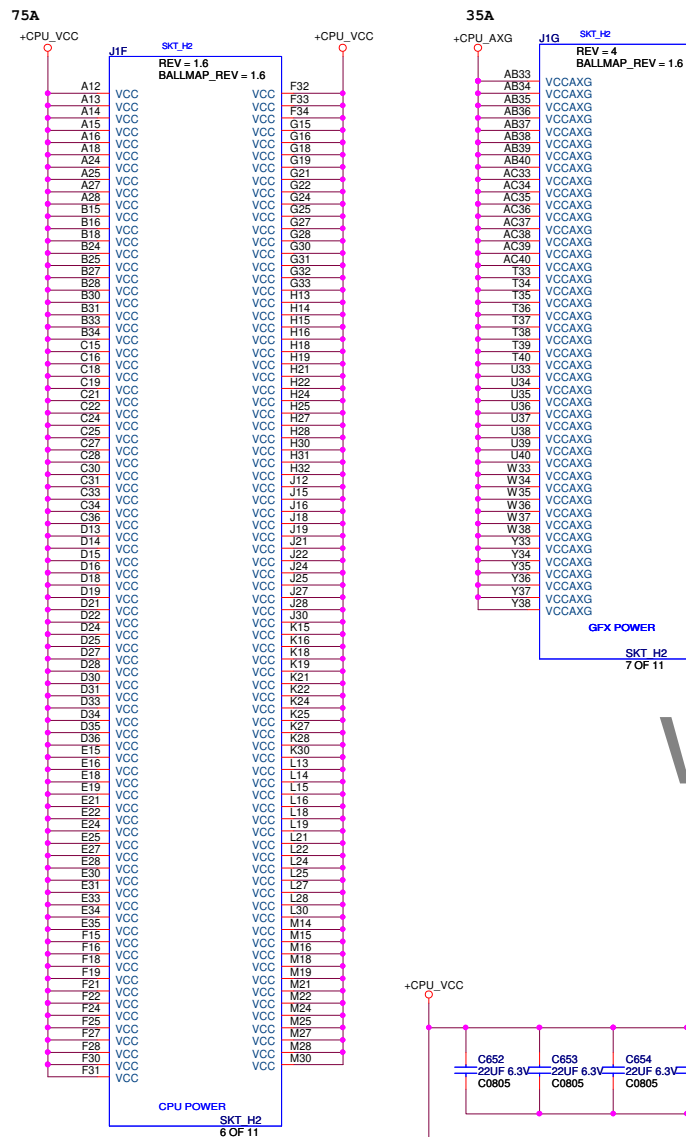


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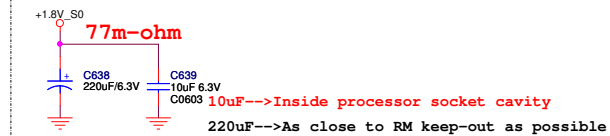


If SM_DRAMRST buffer strength is not enough, need to pop this circuit.

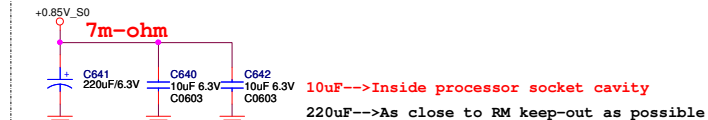
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Circuit diagram NO. <Circuit diagram NO.>	T&I MODEL Lanyard	Rev	M08
Key Component COVER SHEET	PCB NAME XXXXXXXXXX	remark	-remark-
Date Tuesday, May 08, 2012	Sheet 6 of 43		



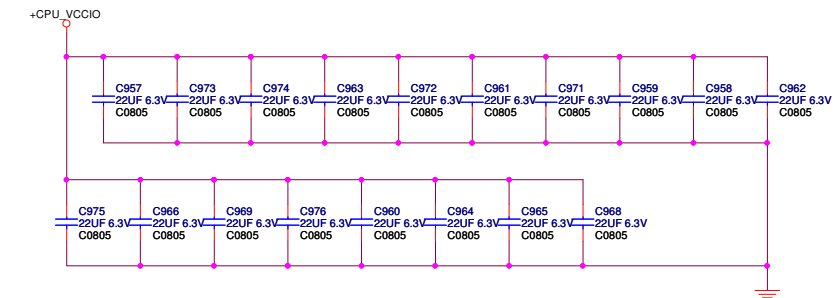
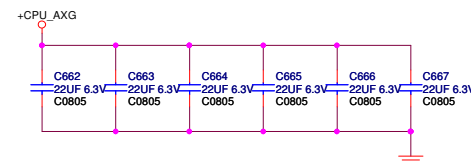
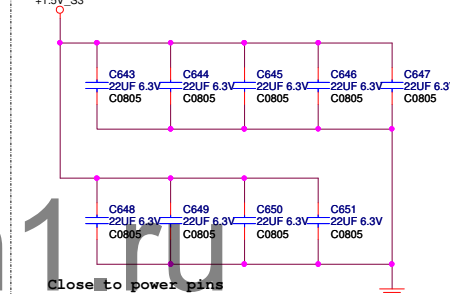
+1.8V_S0-->Decoupling



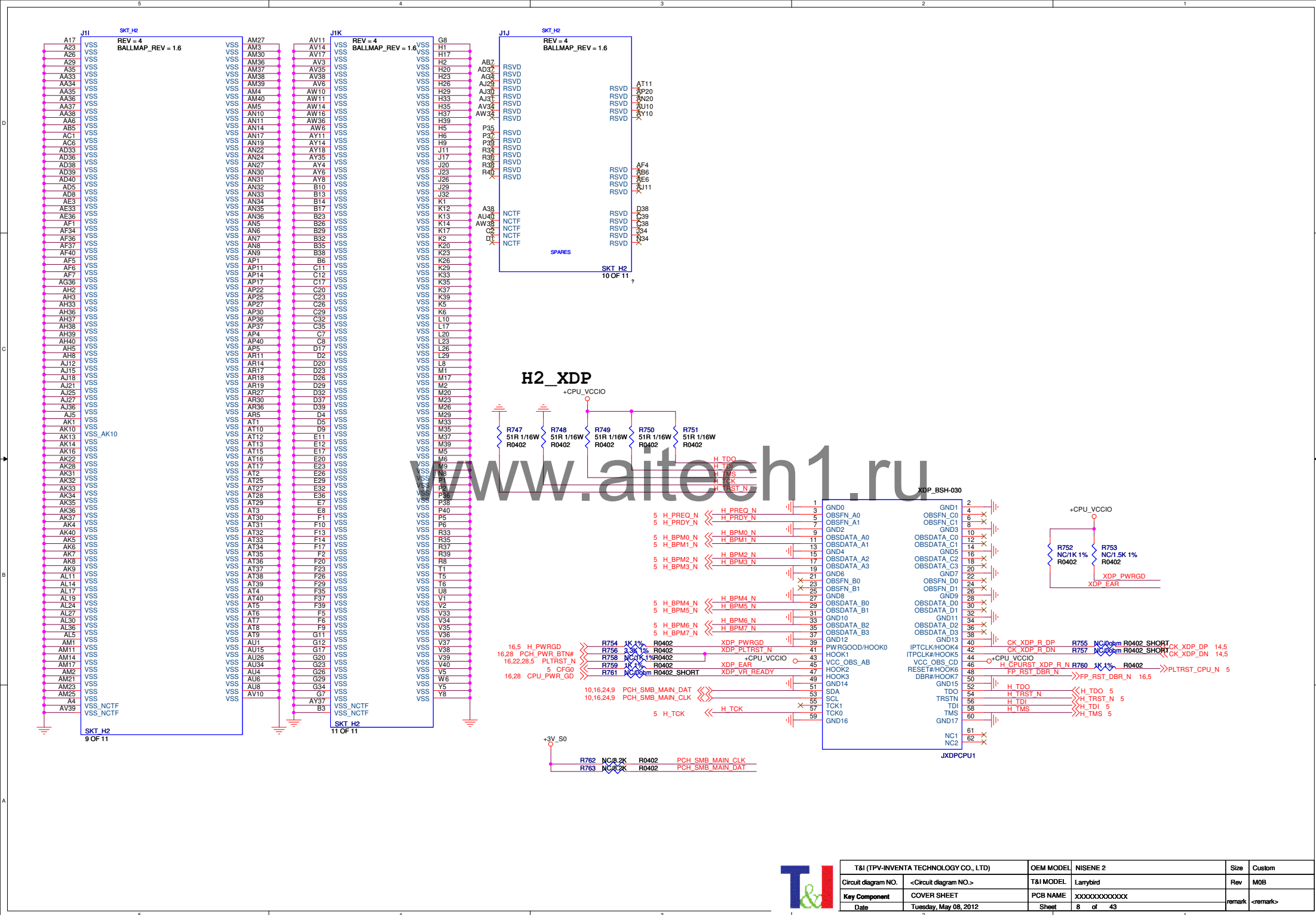
+0.85V_S0-->Decoupling



+1.5V_S0-->Decoupling

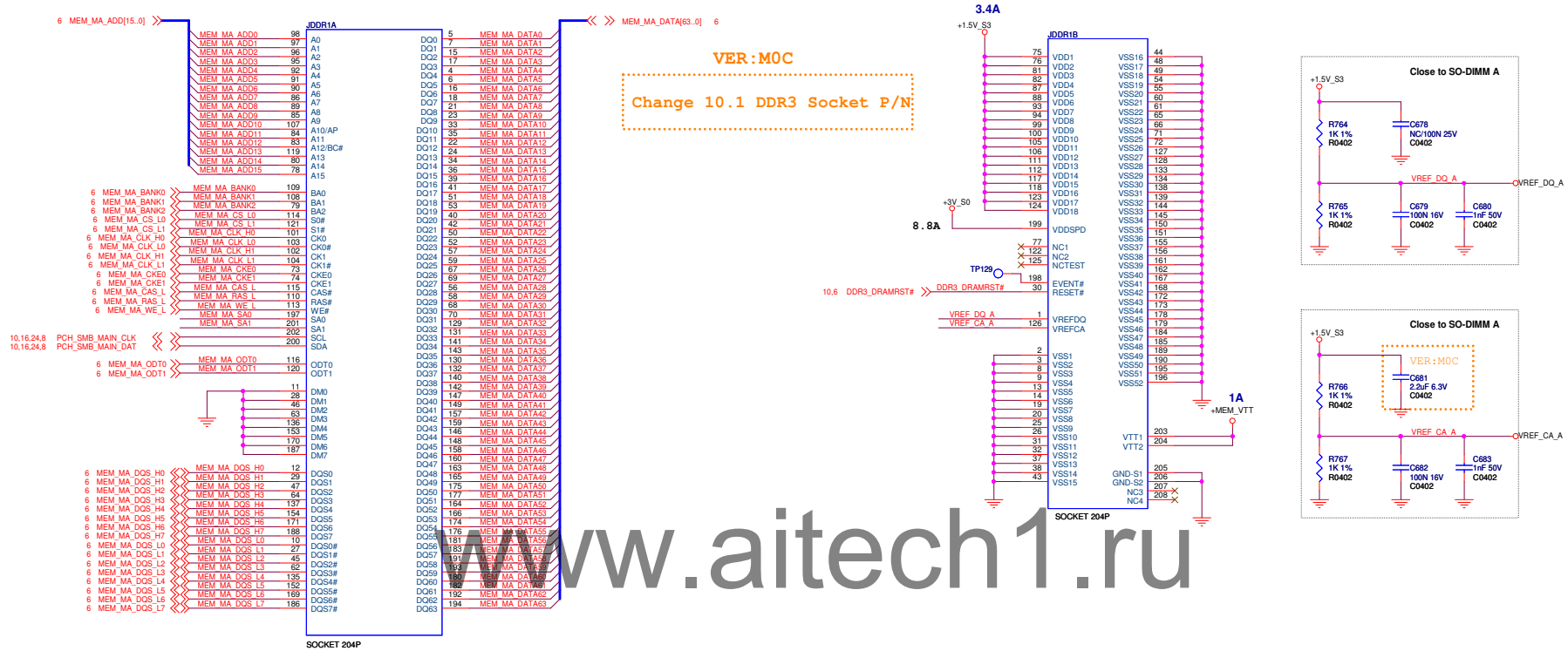


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Tuesday, May 08, 2012	Sheet	7 of 43	<remark>

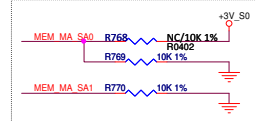


VER:MOB
JDDR1 is change to 10.1mm height

CHA DDR 10.1H(DIMM-1)

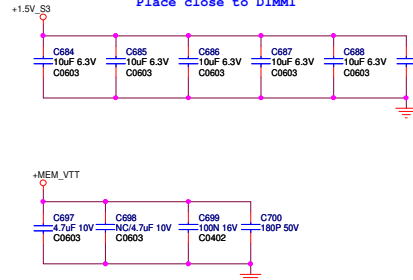


DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

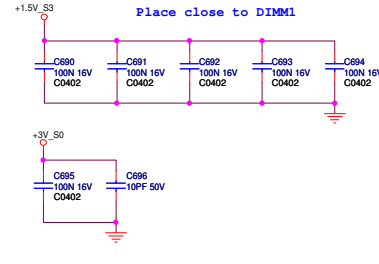


Note:
If SA0 = 0, SA1 = 0
SO-DIMM1 SPD Address is 0xA0
SO-DIMM1 TS Address is 0x30
If SA0 = 1, SA1 = 0
SO-DIMM1 SPD Address is 0xA2
SO-DIMM1 TS Address is 0x32

Place close to DIMM1



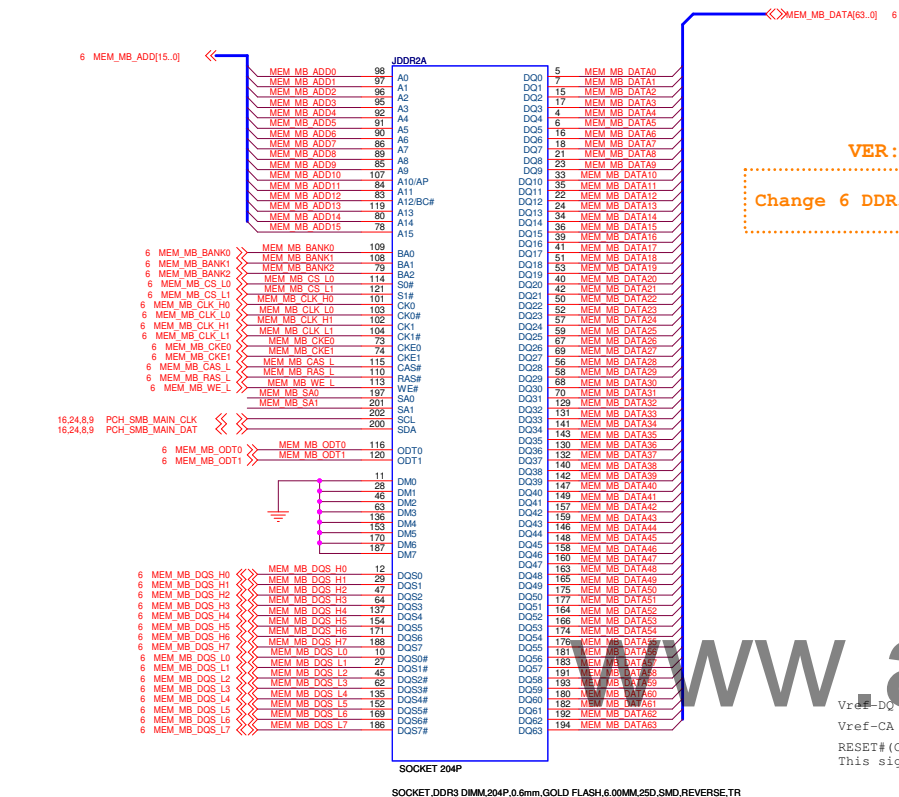
Place close to DIMM1



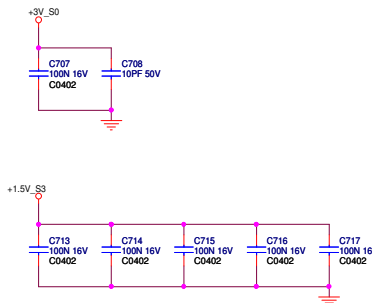
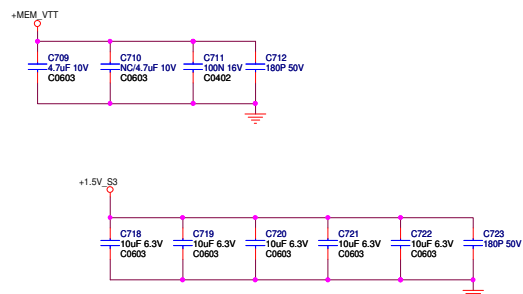
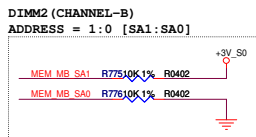
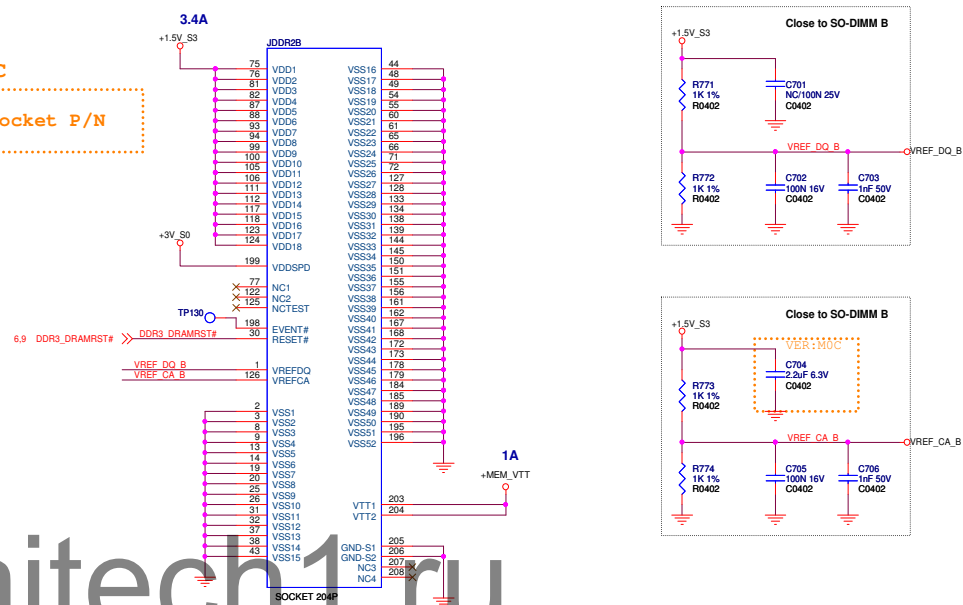
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Circuit diagram NO.	<Circuit diagram NO.>	Lanybird	Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Tuesday, May 08, 2012	Sheet	9 of 43	<remark>

VER:MOB
JDDR1 is change to 6.0mm height

CHB DDR 6.0H(DIMM-2)

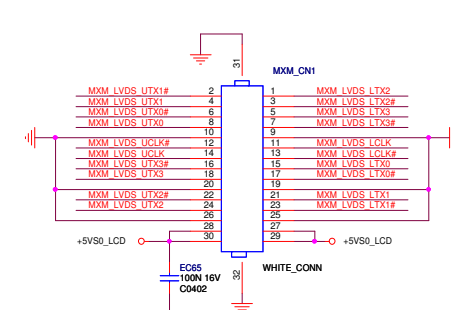
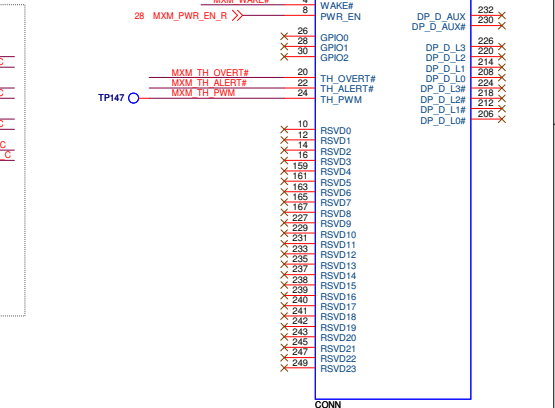


VER:MOB
Change 6 DDR3 Socket P/N



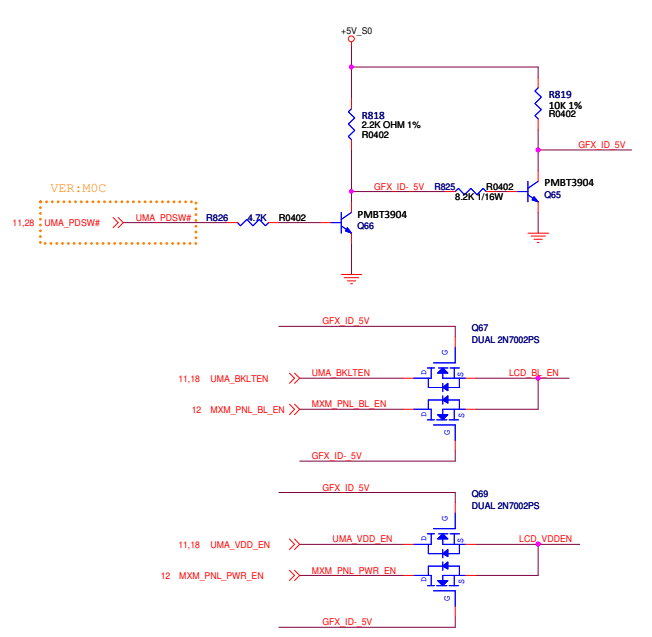
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Circuit diagram NO.	<Circuit diagram NO.>	Lanybird	Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Tuesday, May 08, 2012	Sheet	10 of 43	<remark>

Change MXM connector P/N

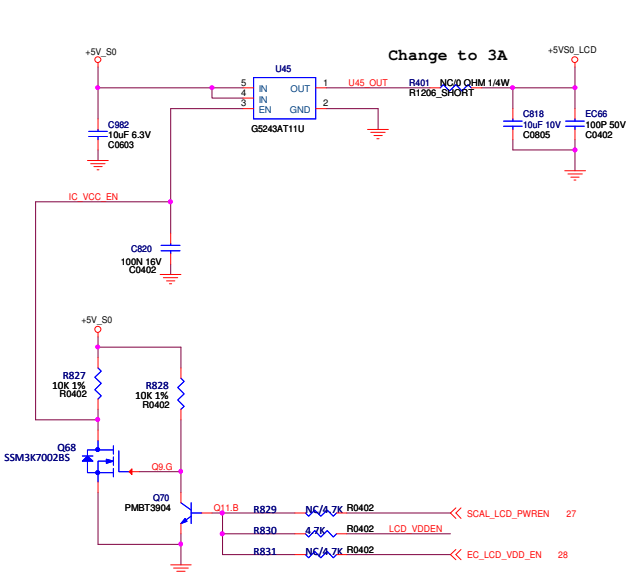


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
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Date	Tuesday, May 08, 2012	Sheet	12 of 43		

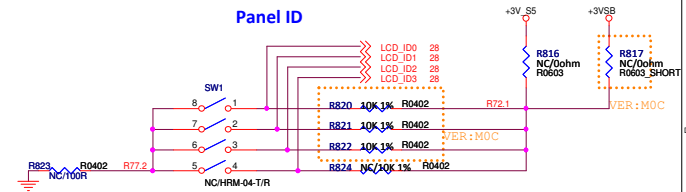
MXM & UMA BACKLIGHT ENABLE AUTO SELECT



LCD POWER ENABLE

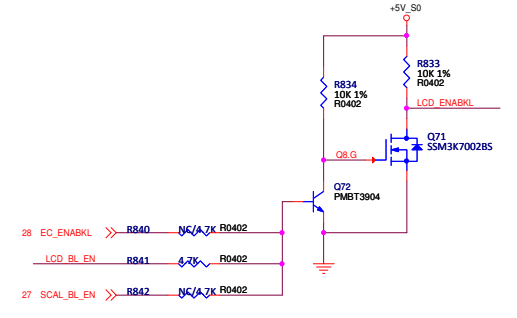


Panel ID



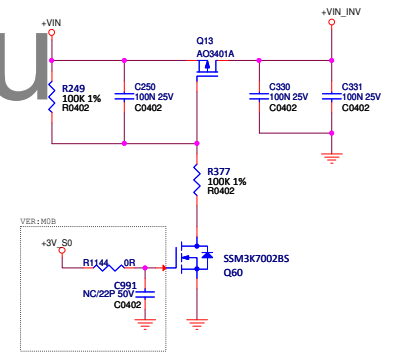
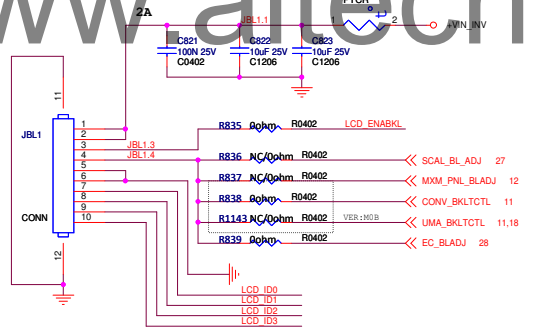
ID3	ID2	ID1	ID0	Panel
0	0	0	0	Samsung
0	0	0	1	LG
0	0	1	0	CMI
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	

BACKLIGHT ENABLE

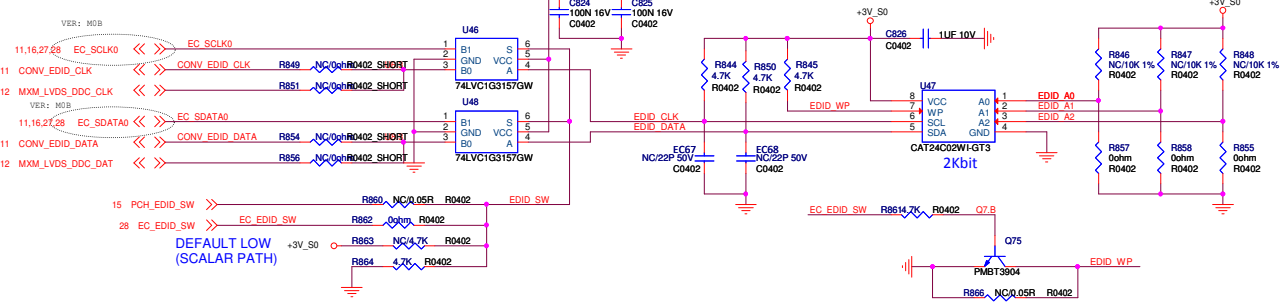


CONVERTER CONNECTOR

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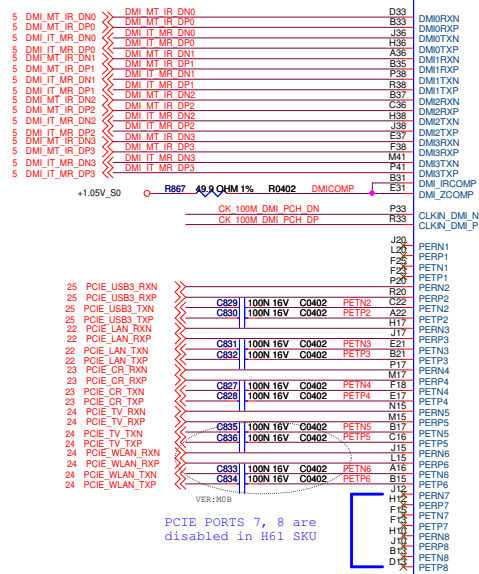


EDID

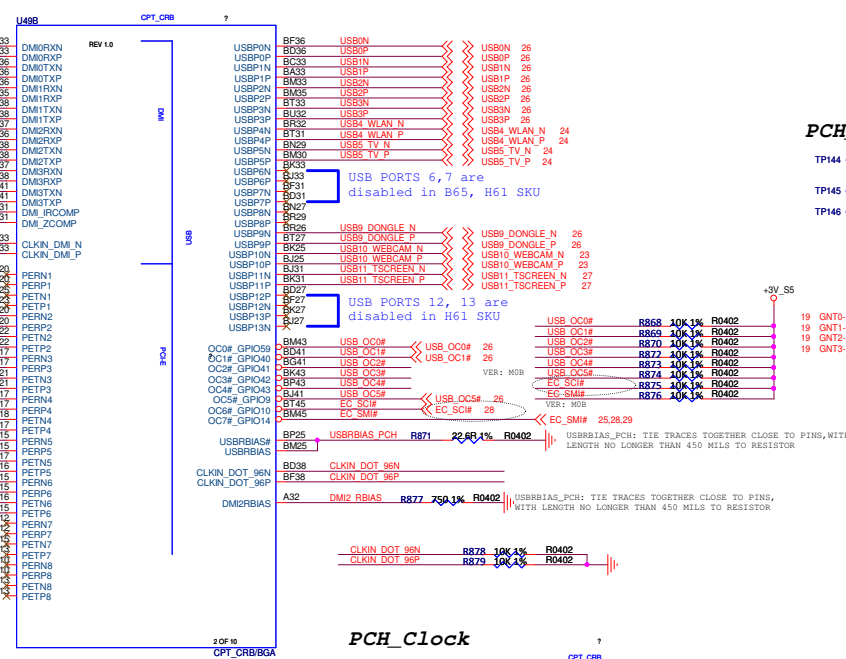
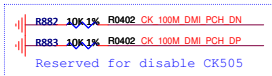


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark	<remark>
Date	Tuesday, May 06, 2012	Sheet	13 of 43	

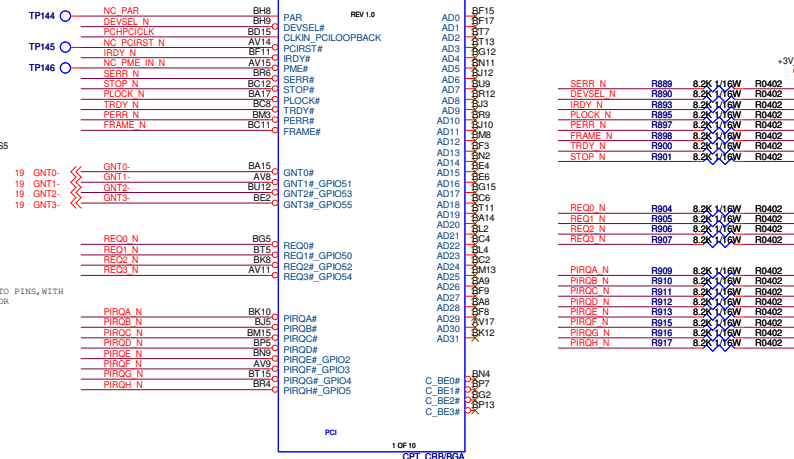
PCH DMI/PCIE/USB



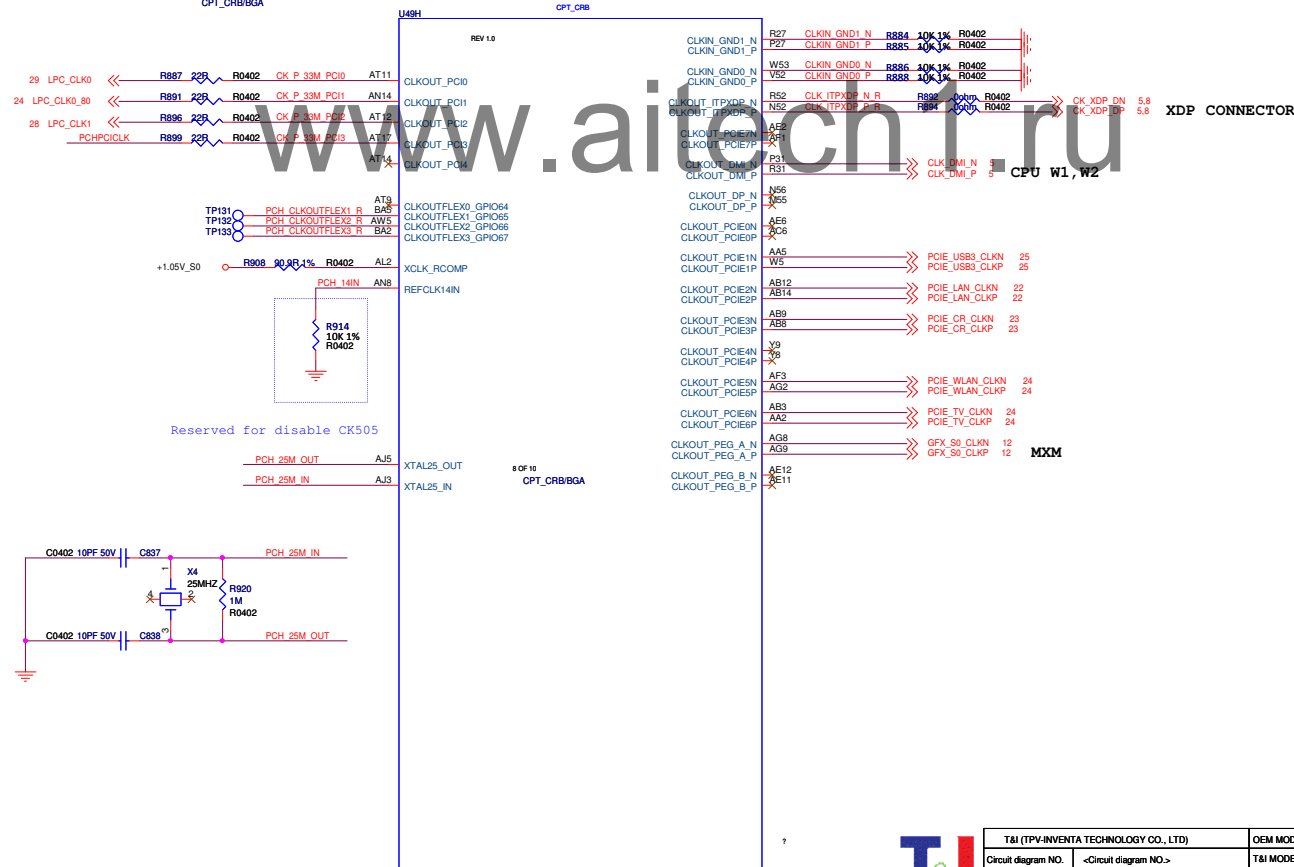
PCIE PORTS 7, 8 are disabled in H61 SKU



PCH_PCI



PCH_Clock



TAI (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	TAI MODEL	Lambrdr	Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark	<remark>
Date	Tuesday, May 08, 2012	Sheet	14 of 43		

PCH SATA

PCH_MEPWROK:
1) .V_1P05_ME
2) .PCH_SLP_A

Not available in Mobile & Desktop

PCH_EDID_SW

BOOT_BLK_WR_EN

PCH_CONFIG Recovery

PCH_GPIO22

R935, R331, R936 -- Normal (Default)

R935, R1026 -- CONFIGURE

PCH_GPIO22

PCH_GPIO22

PCH_GPIO22

PCH_GPIO22

PCH_GPIO22

PCH_GPIO22

PCH_GPIO22

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PCH_GPIO22

PCH_GPIO22

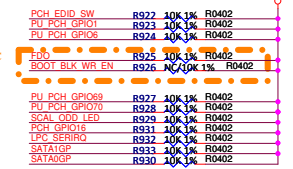
PCH_GPIO22

3.5" HDD

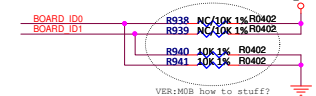
mSATA

ODD

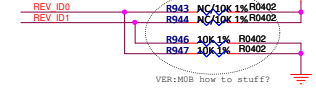
Pull HIGH for PCH



BOARD ID

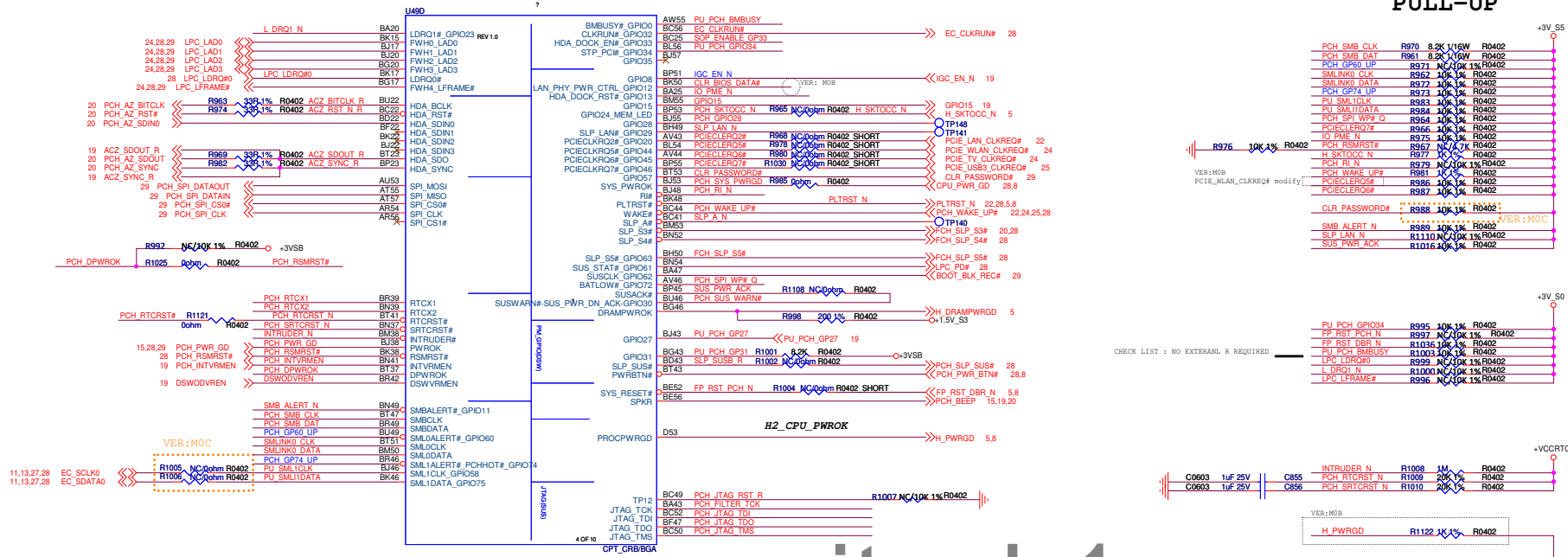


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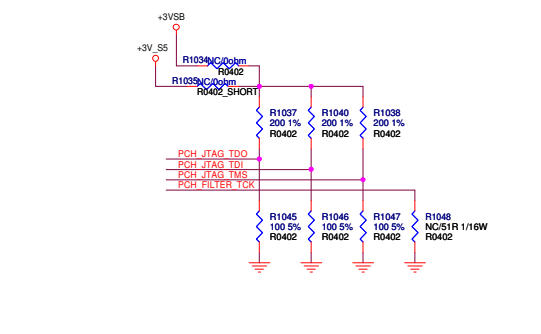
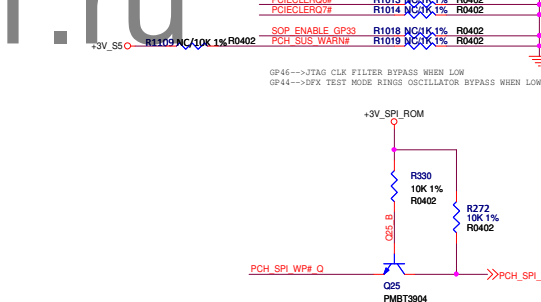
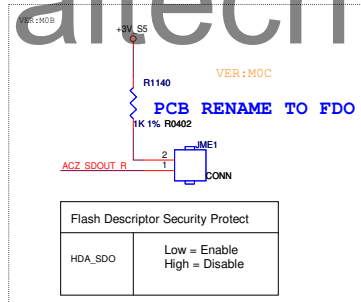


PCH_HDA/SPI/LPC/MISC/

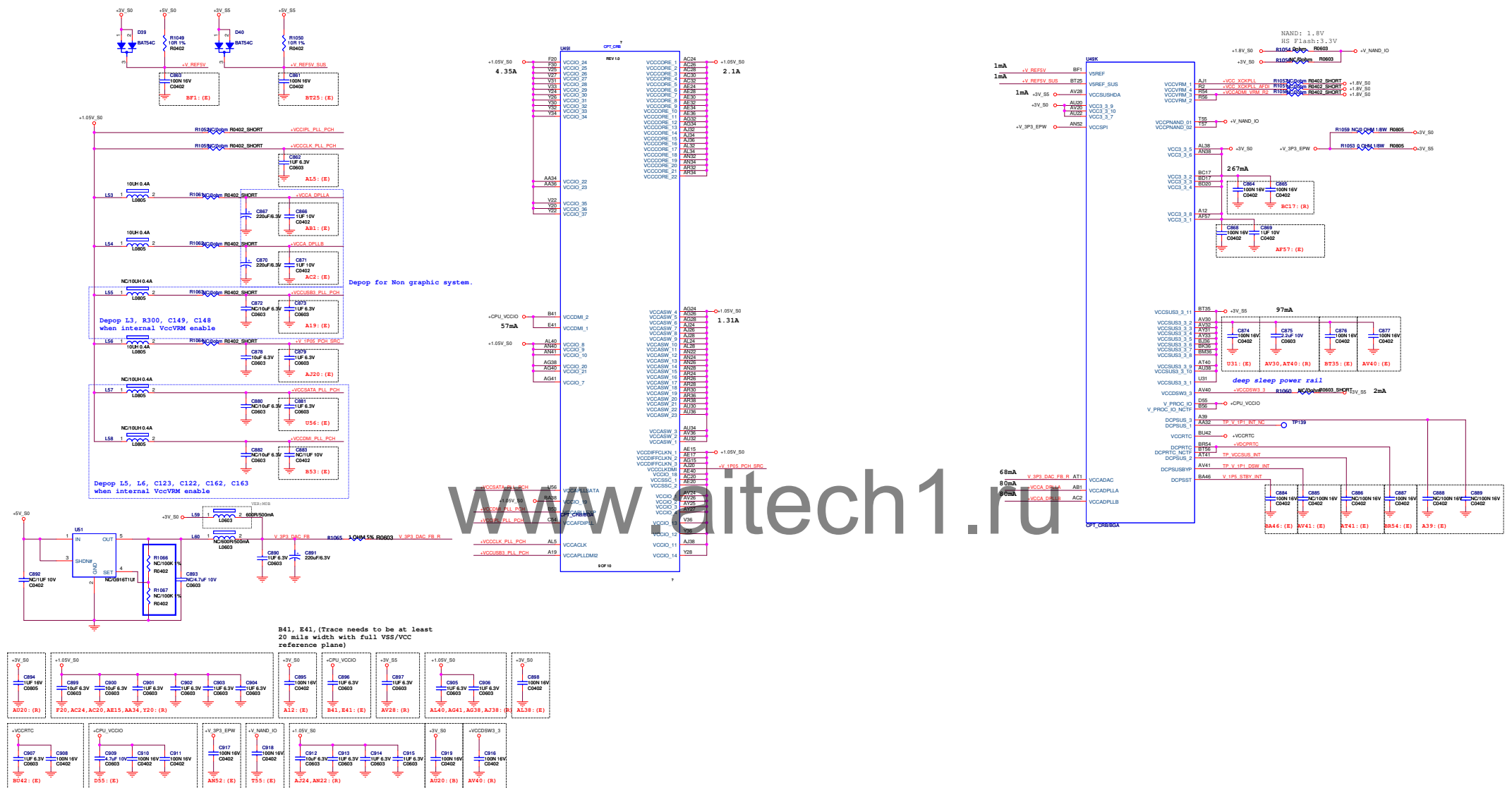
PULL-UP



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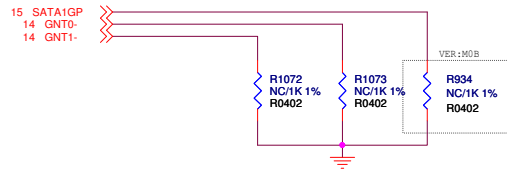


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	Circuit diagram NO.		Rev	MOB
Key Component	COVER SHEET	T&I MODEL	Lanybird	
		PCB NAME	XXXXXXXXXXXX	remark
Date	Tuesday, May 06, 2012	Sheet	16 of 43	remark



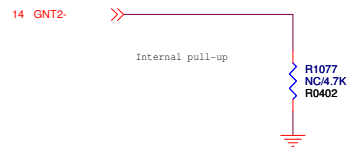
T&I (TPV INVENTA TECHNOLOGY CO., LTD)		DEM MODEL	MEBENE 2	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	TEI MODEL	Lanyard	Rev	MSB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	Drawn	re-mark
Date	Tuesday, May 08, 2012	Sheet	17 of 43		

CP REQUIRED STRAPS

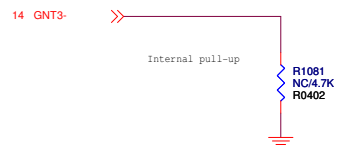


BOOT select straps

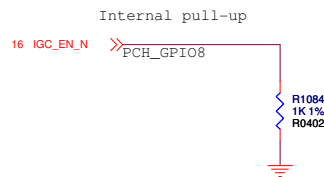
GNT1-	SATA1GP	Boot device
0	0	LPC
1	0	PCI
1	1	SPI(Default)



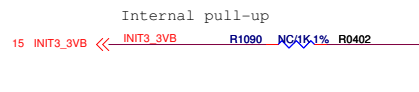
DMI AC/DC MODE
0 : AC
1 : DC *



Topblock swap override when pull-low
Signal has a weak internal pull-up

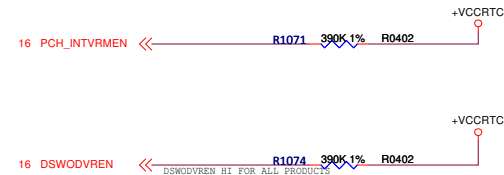


GPIO8
0 : Integrated Clocking Enable (FCIM) *
1 : Buffer Through Mode Enable (BTM)



INT3_3V#
0 : ??????????????
1 : ?????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

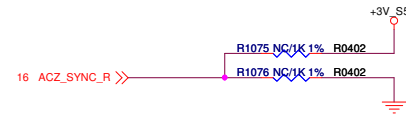


INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

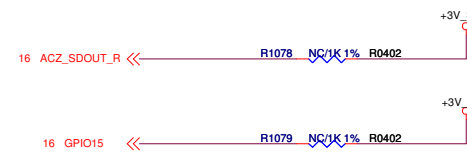
This signal enables the internal Deep Sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.



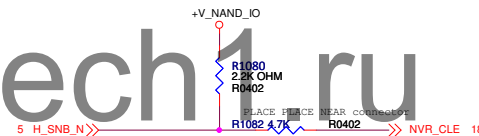
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

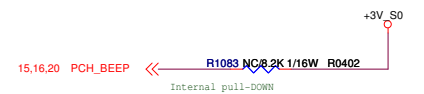
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



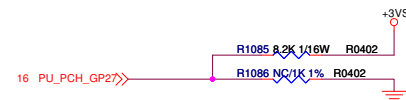
GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



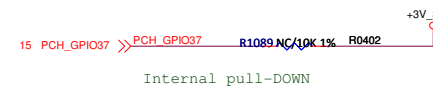
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



In Deep Sleep Power Well.
If not used, require a weak pull-up (8.2k-10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high



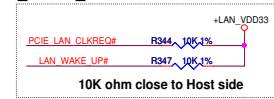
Cougar point EDS PAGE:93 This signal should not be pull high



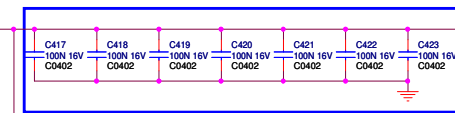
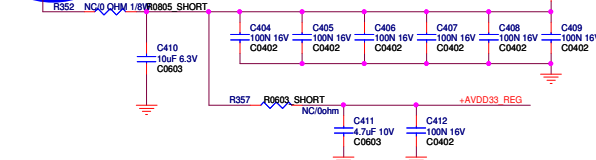
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark	<remark>
Date	Tuesday, May 08, 2012	Sheet	19 of 43		

GIGA LAN

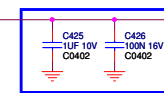
PCIE_LAN_CLKREQ# Connect To SB
LAN_WAKE_UP# Connect To SB



+LAN3V_DUAL



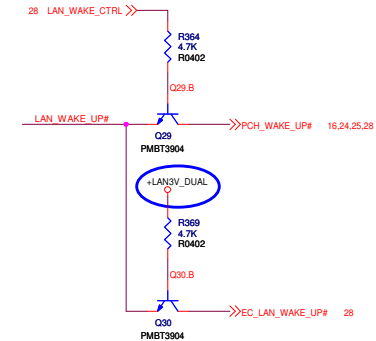
Close To 8171E



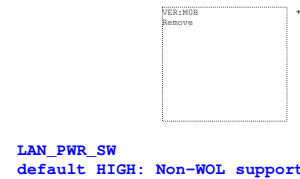
	Link LED (left)	Speed LED (right)
Test	Link/Data Transfer	Link/Data Transfer
10M bit	Yellow (solid)/Yellow (blink)	Off (no color)/Off (no color)
S0	Yellow (solid)/Yellow (blink)	Off (no color)/Off (no color)
S3		
S4		
S5		

	Link LED (left)	Speed LED (right)
Test	Link/Data Transfer	Link/Data Transfer
100M bit	Yellow (solid)/Yellow (blink)	Orange (solid)/Orange (solid)
S0	Yellow (solid)/Yellow (blink)	Orange (solid)/Orange (solid)
S3		
S4		
S5		

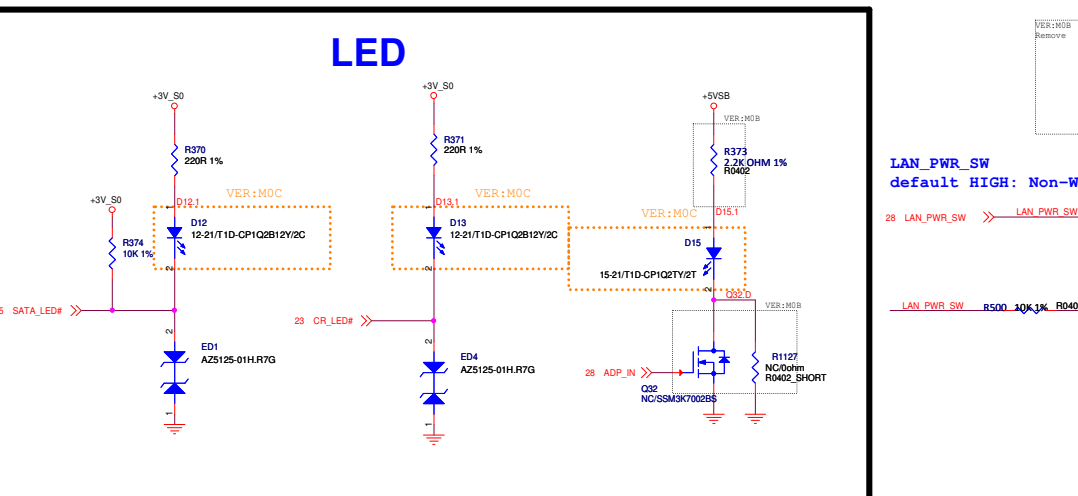
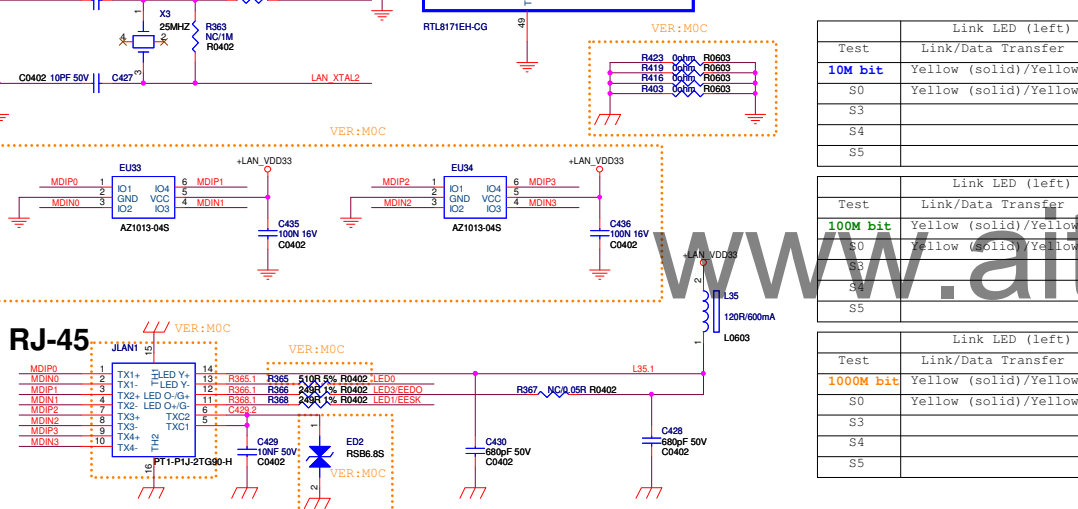
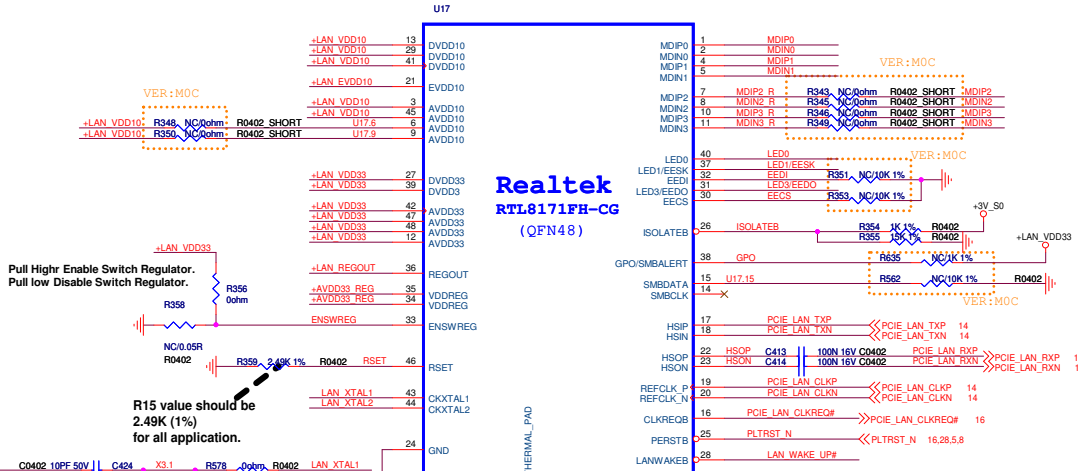
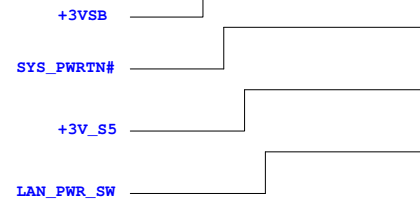
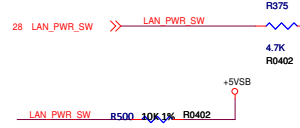
	Link LED (left)	Speed LED (right)
Test	Link/Data Transfer	Link/Data Transfer
1000M bit	Yellow (solid)/Yellow (blink)	Green (solid)/Green (solid)
S0	Yellow (solid)/Yellow (blink)	Green (solid)/Green (solid)
S3		
S4		
S5		



LAN POWER SWITCH

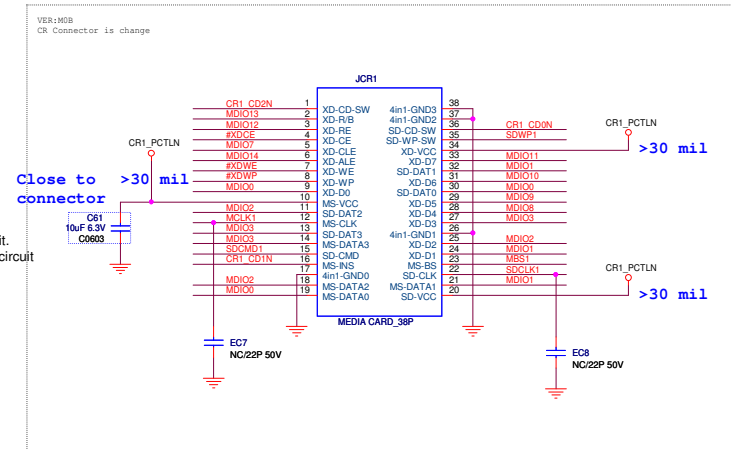


LAN_PWR_SW default HIGH: Non-WOL support

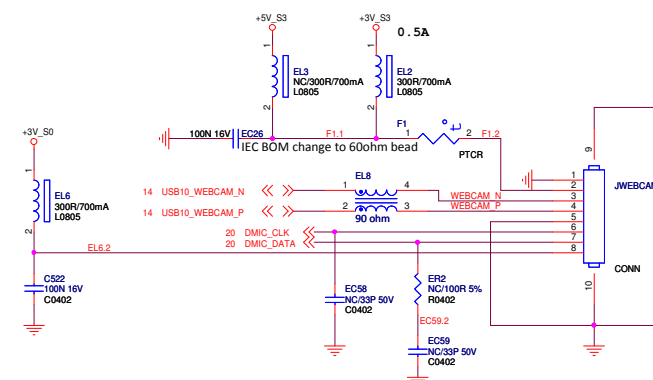
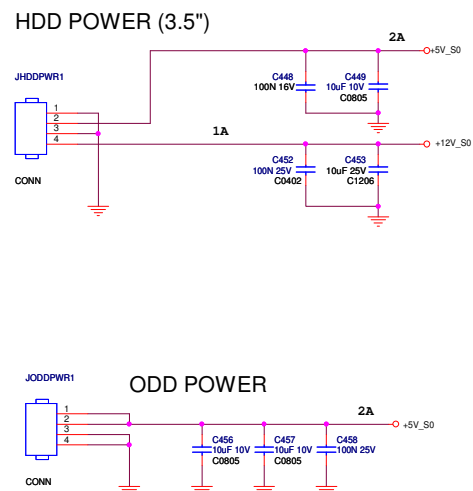


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NIENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
COVER SHEET		PCB NAME	XXXXXXXXXXXX	MOB
Date	Tuesday, May 06, 2012	Sheet	22 of 43	remark

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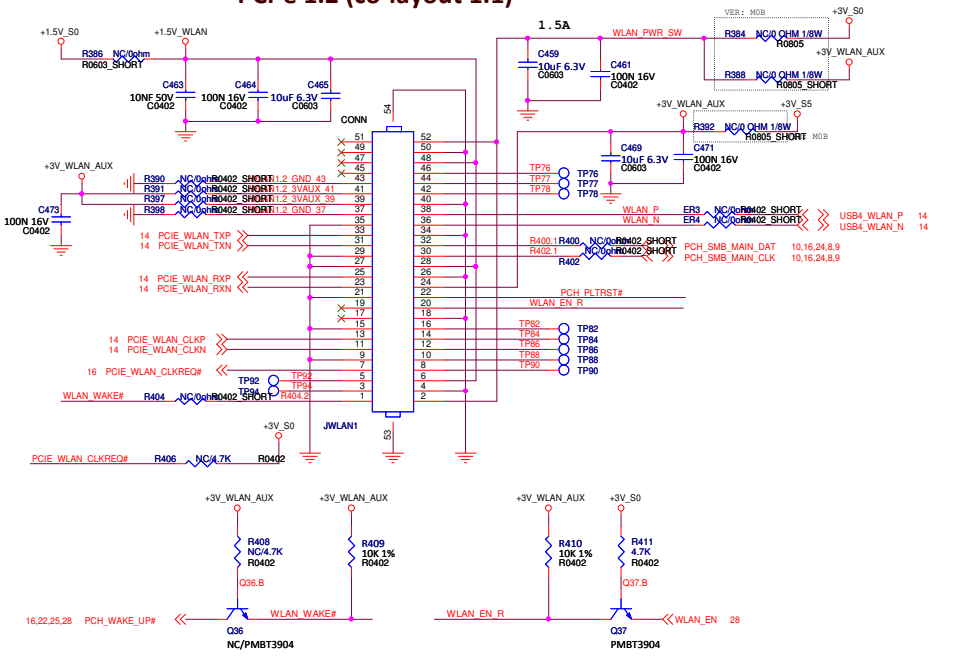
WEB CAM



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lamy&rd		Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX			
Date	Tuesday, May 08, 2012	Sheet	23 of 43		remark	<remark>

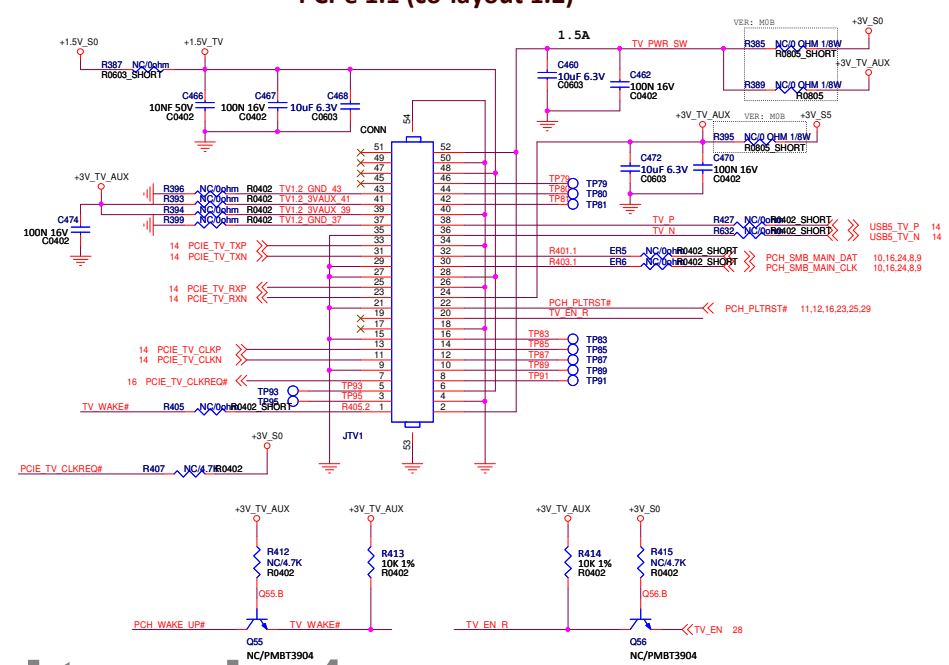
MINI PCI-E WLAN & BT

PCI-e 1.2 (co-layout 1.1)

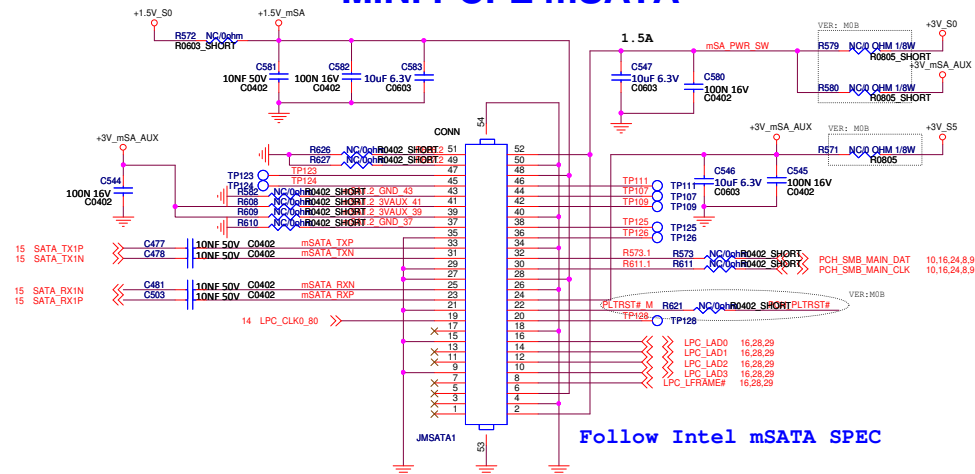


MINI PCI-E TV CARD

PCI-e 1.1 (co-layout 1.2)

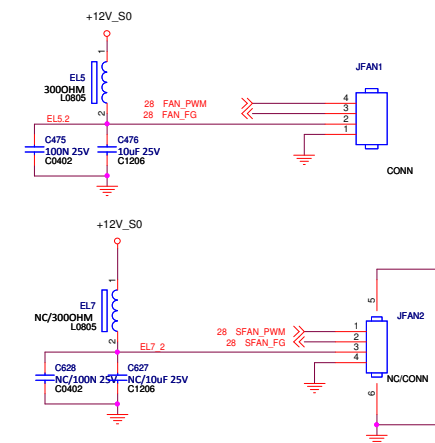


MINI PCI-E mSATA



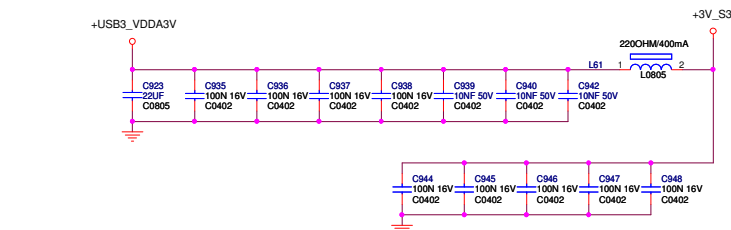
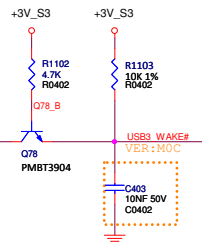
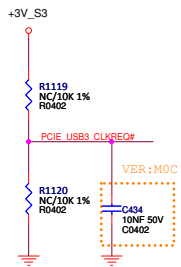
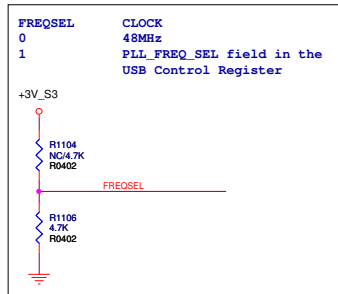
Follow Intel mSATA SPEC

CPU Linear FAN Control



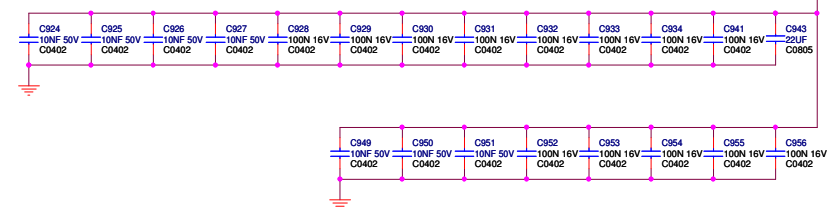
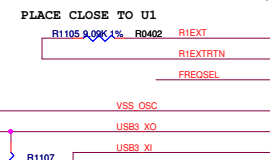
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark	<remark>
Date	Tuesday, May 08, 2012	Sheet	24 of 43		

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POPULATE PULLDOWN IF I2C EEPROM
NOT USED AND DO NOT POPULATE
PULLUP.

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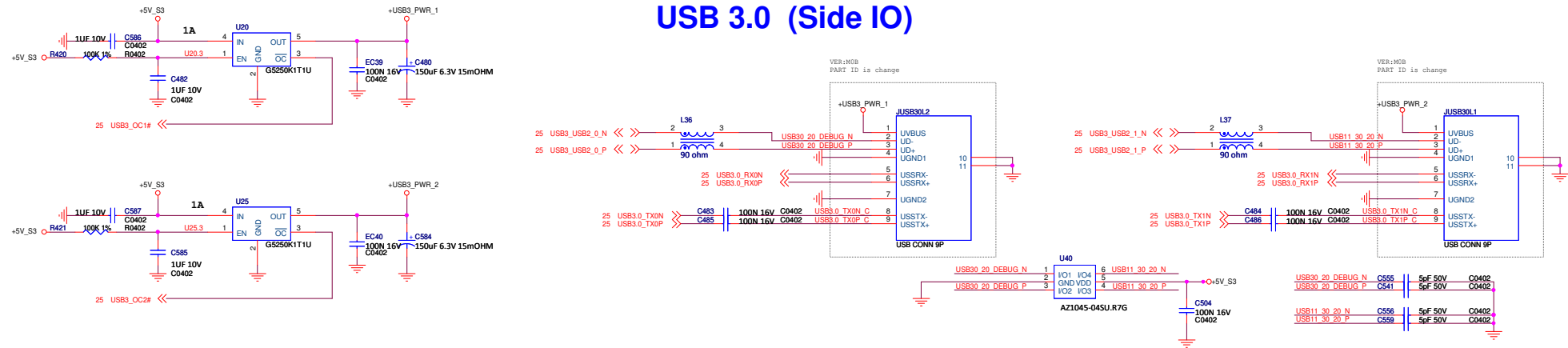


TUSB7320

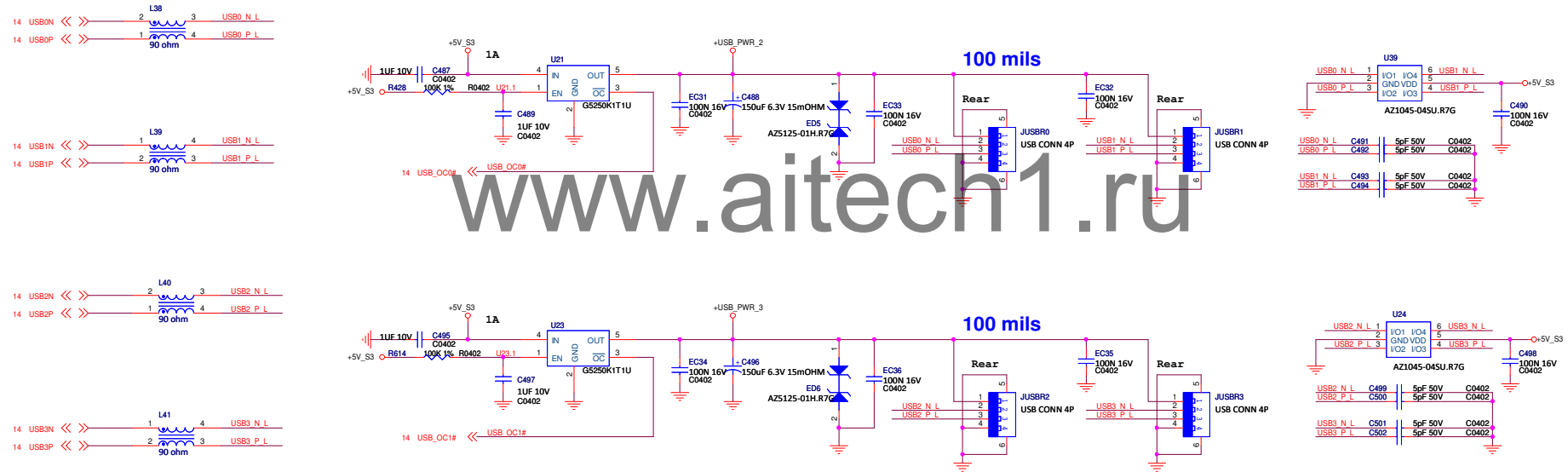


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Tuesday, May 08, 2012	Sheet	25 of 43	<remark>

USB 3.0 (Side IO)



USB 2.0 (Rear IO)

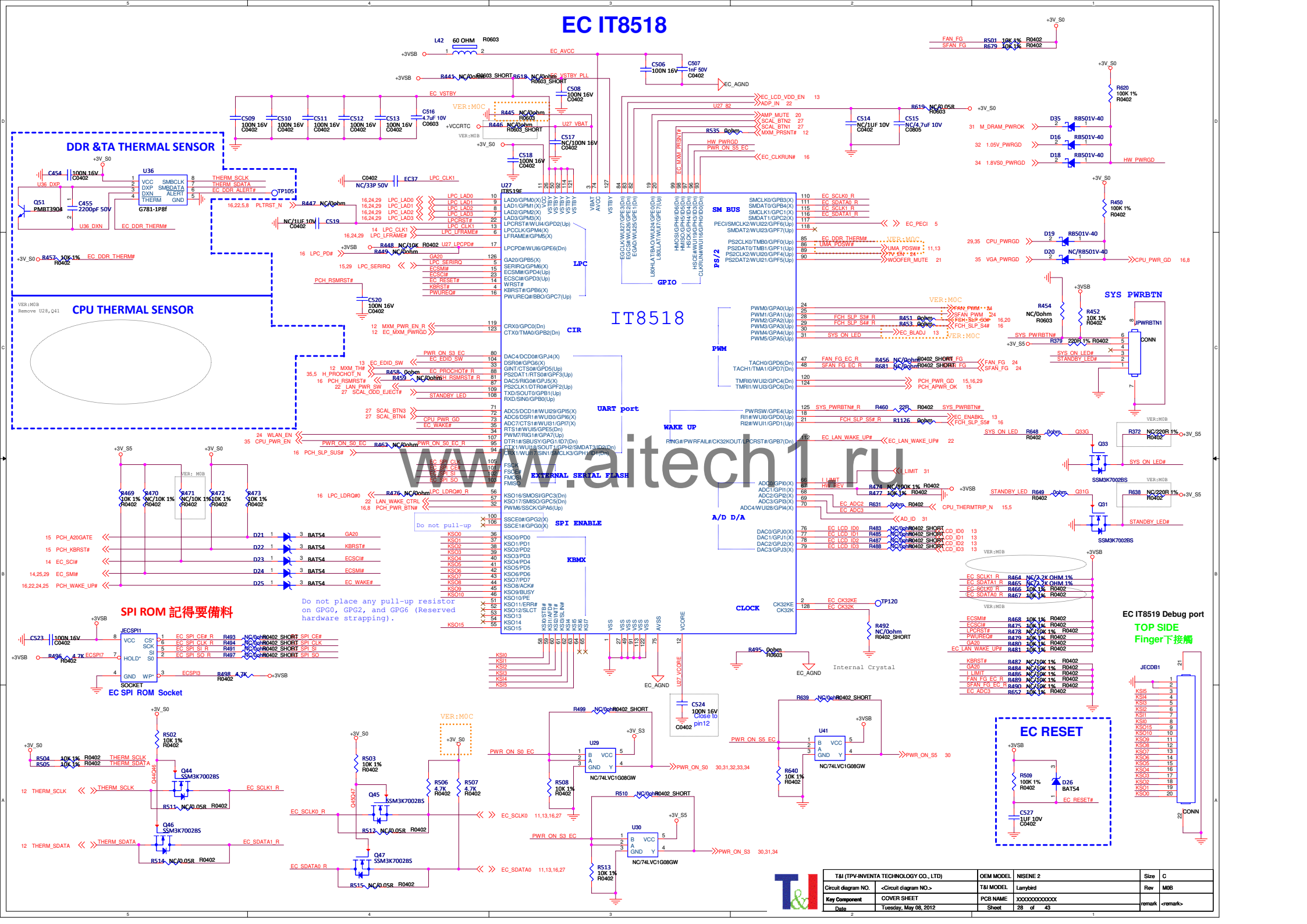


USB 2.0 (Dongle)



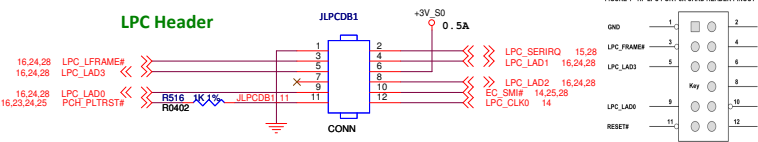
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lambybird	Rev
COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark	<remark>
Date	Tuesday, May 08, 2012	Sheet	26 of 43	

EC IT8518



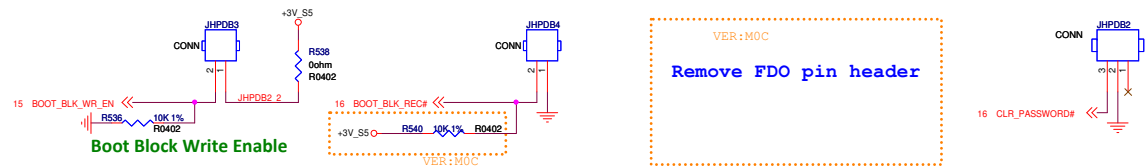
HP LPC DEBUG PIN HEADER

LPC Header

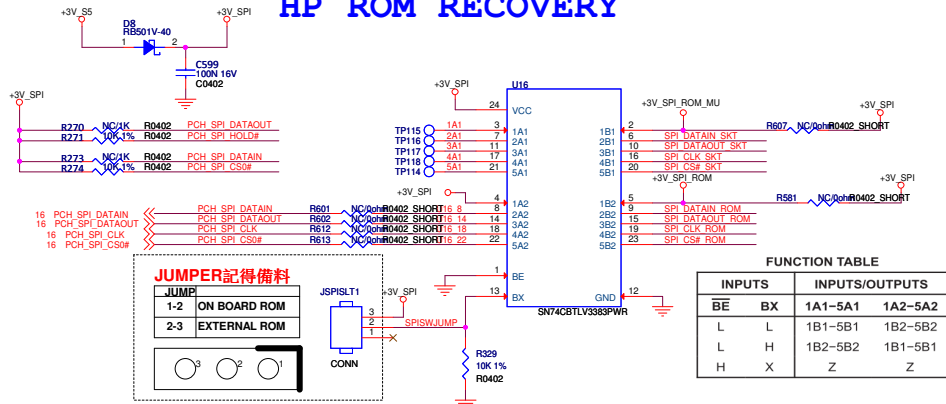


HP Header	Function
FDO	default: Low Jumper:High
CLR_PASSWD#	default: high Jumper:low
BOOT_BLK_REC#	default:high Jumper:low

HP REQUEST PIN HEADER



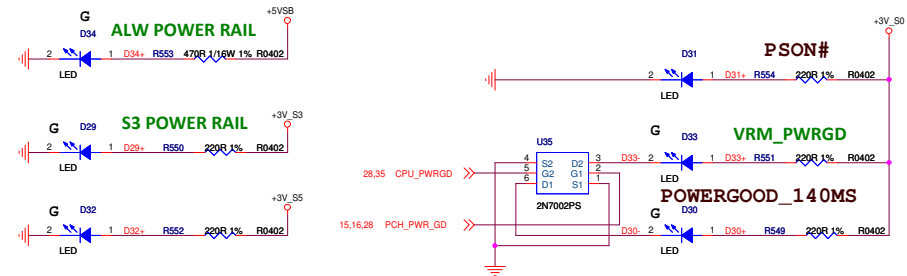
HP ROM RECOVERY



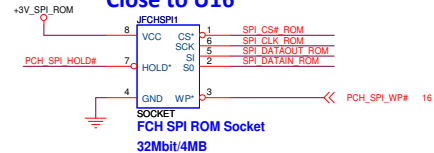
FUNCTION TABLE			
INPUTS		INPUTS/OUTPUTS	
BE	BX	1A1-5A1	1A2-5A2
L	L	1B1-5B1	1B2-5B2
L	H	1B2-5B2	1B1-5B1
H	X	Z	Z

AUX_POWER

HP Indicator LED



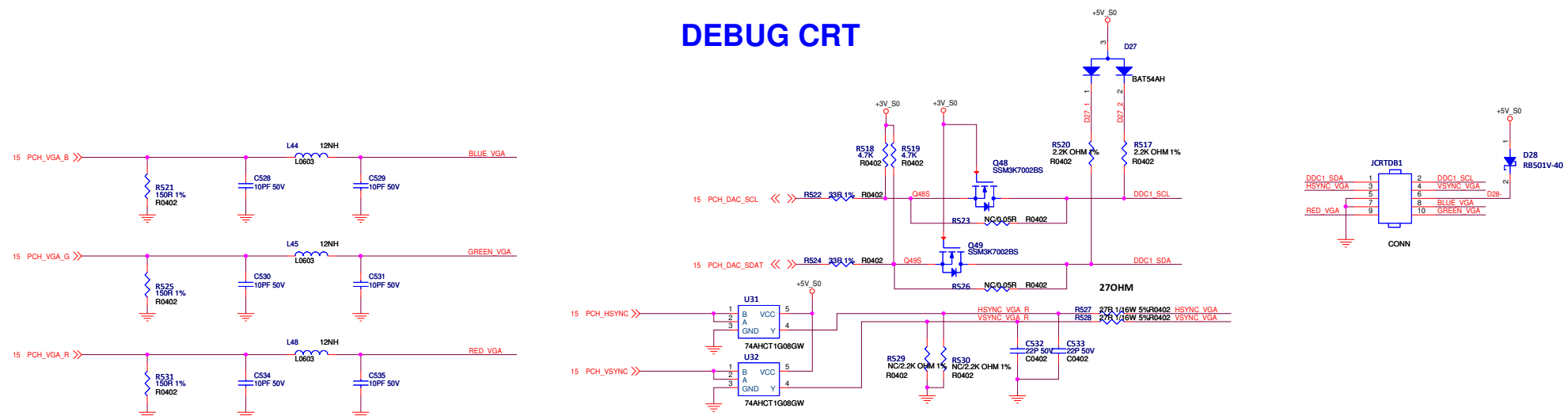
Close to U16



ROM Recovery Header

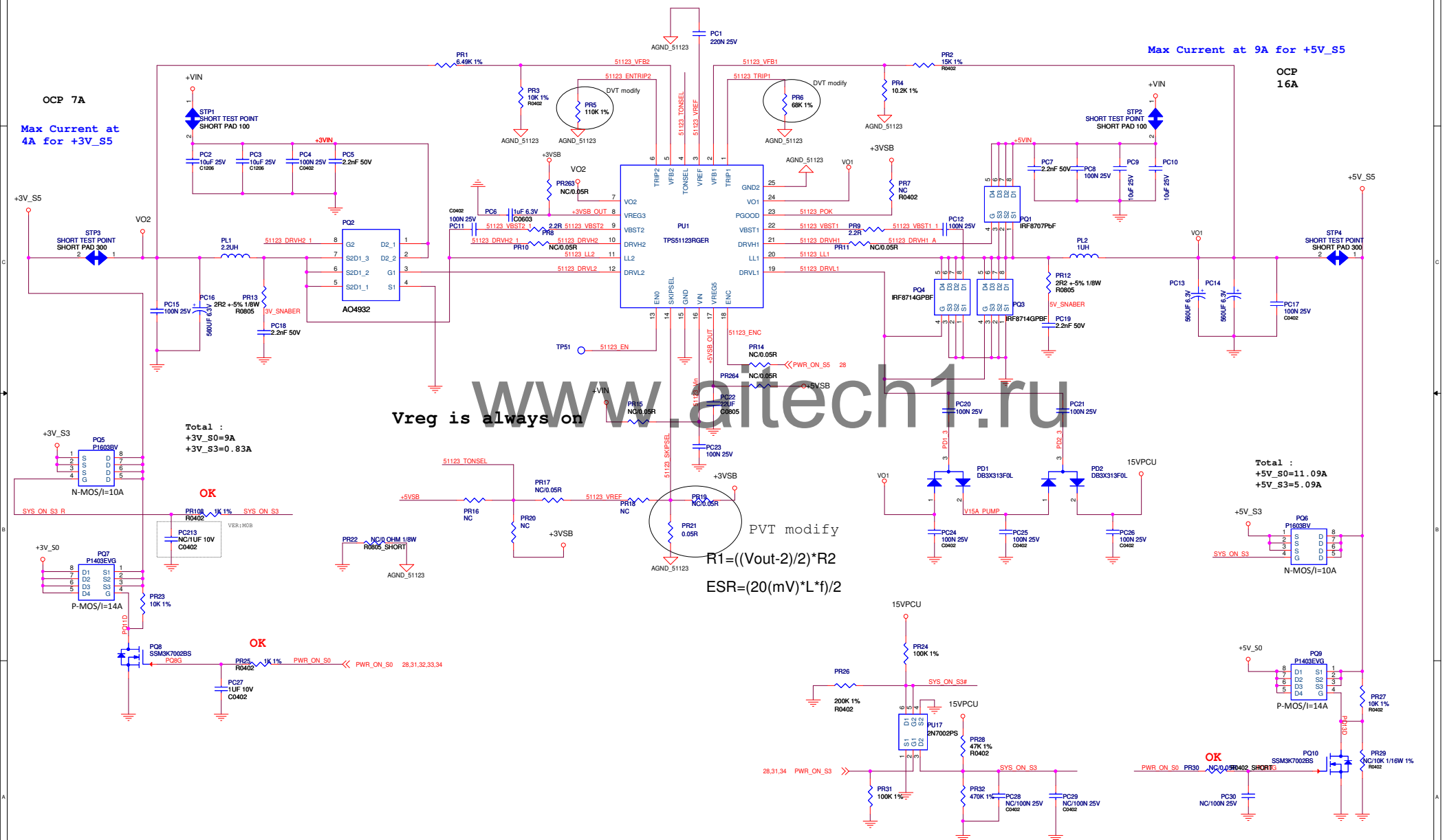


DEBUG CRT



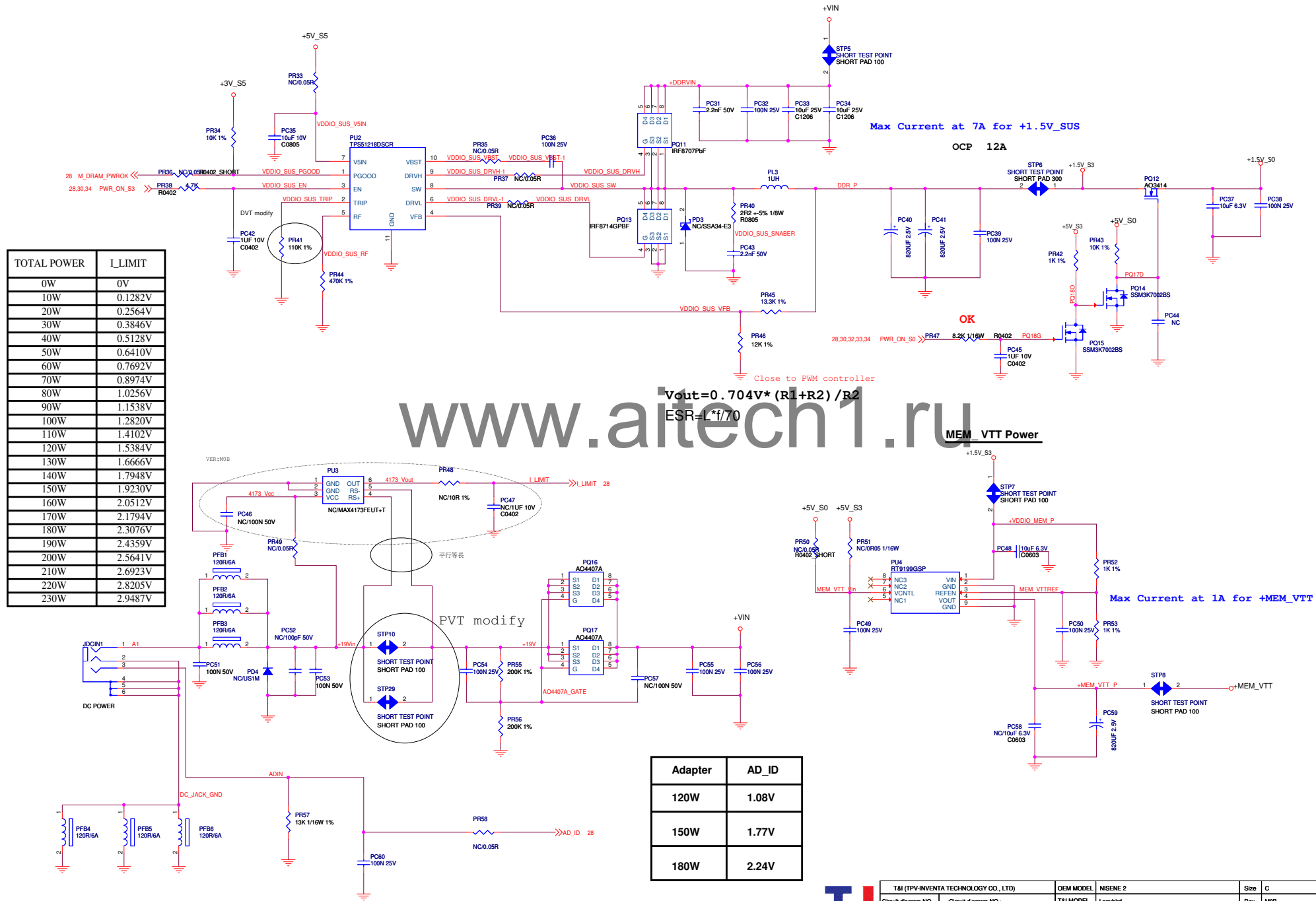
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lambird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Tuesday, May 06, 2012	Sheet	29 of 43	<remark>

SYSTEM +3V_S5/+3V_S3/+3V_S0 +5V_S5/+5V_S3/+5V_S0

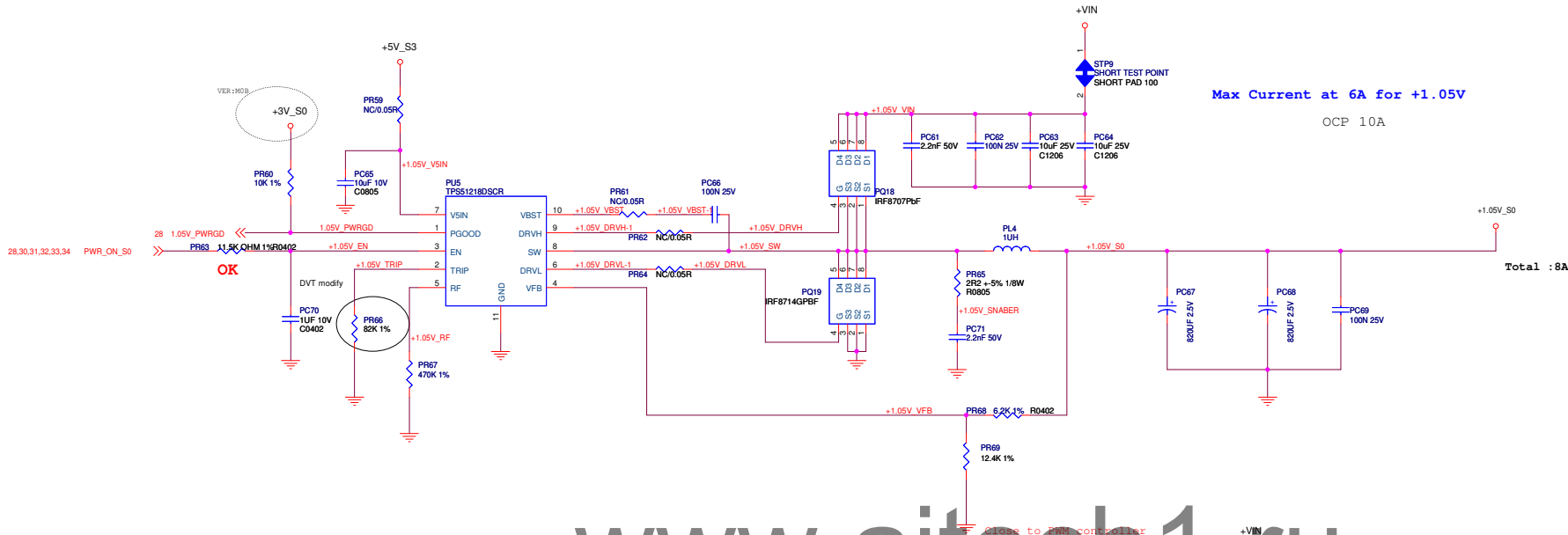


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lambird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	remark
Date	Tuesday, May 06, 2012	Sheet	30 of 43	remark

+1.5V_SUS, MEM_VTT, DC-IN

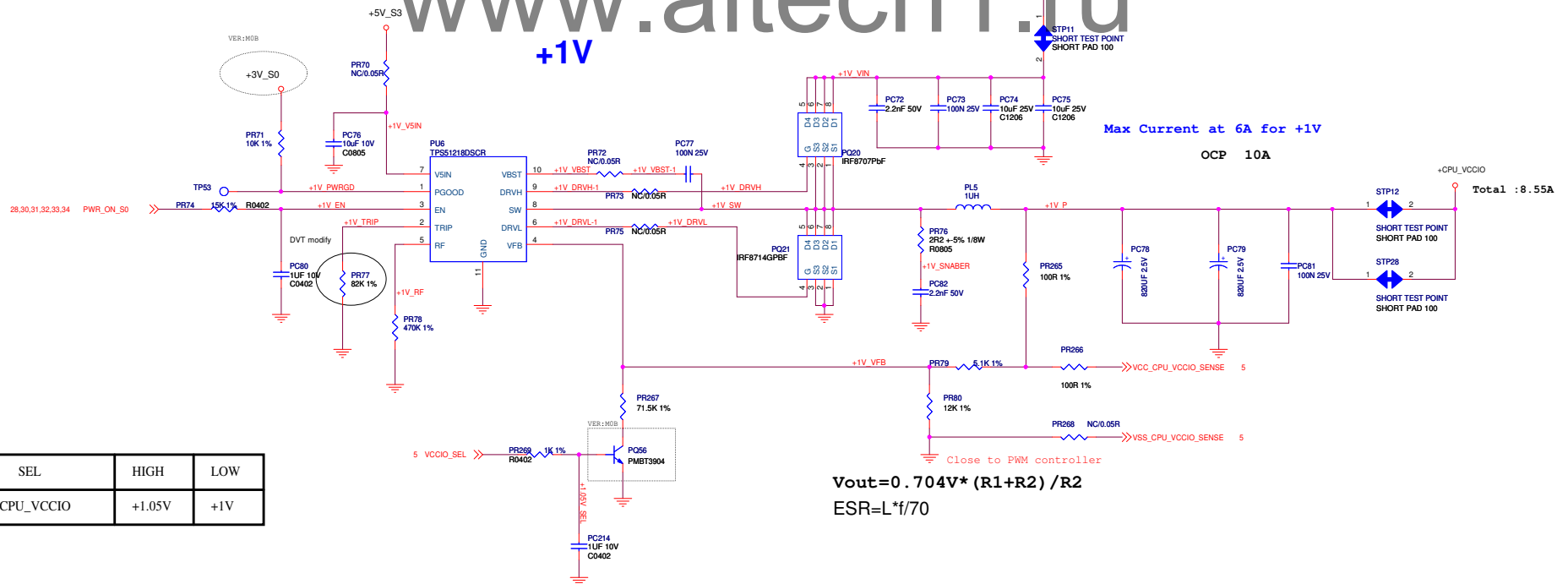


+1.05V



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+1V



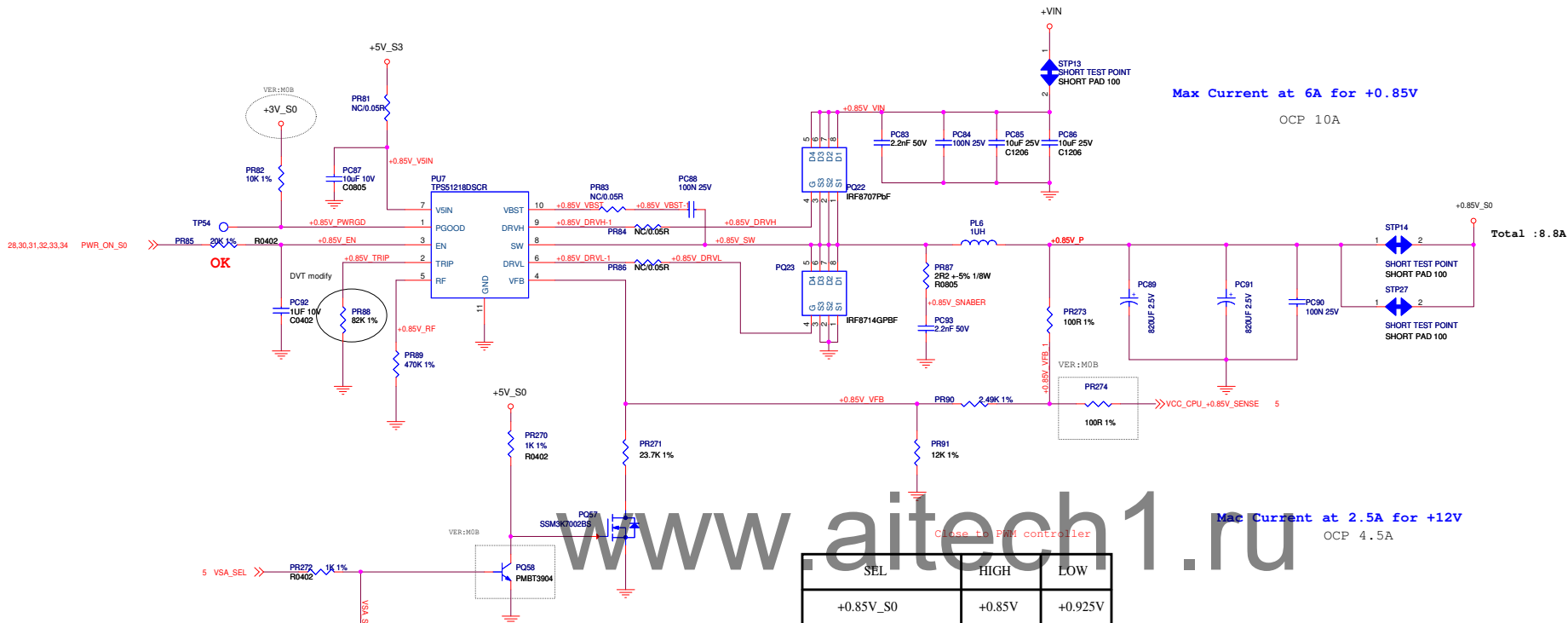
$$V_{out} = 0.704V * (R1 + R2) / R2$$
$$ESR = L * f / 70$$

SEL	HIGH	LOW
+CPU_VCCIO	+1.05V	+1V

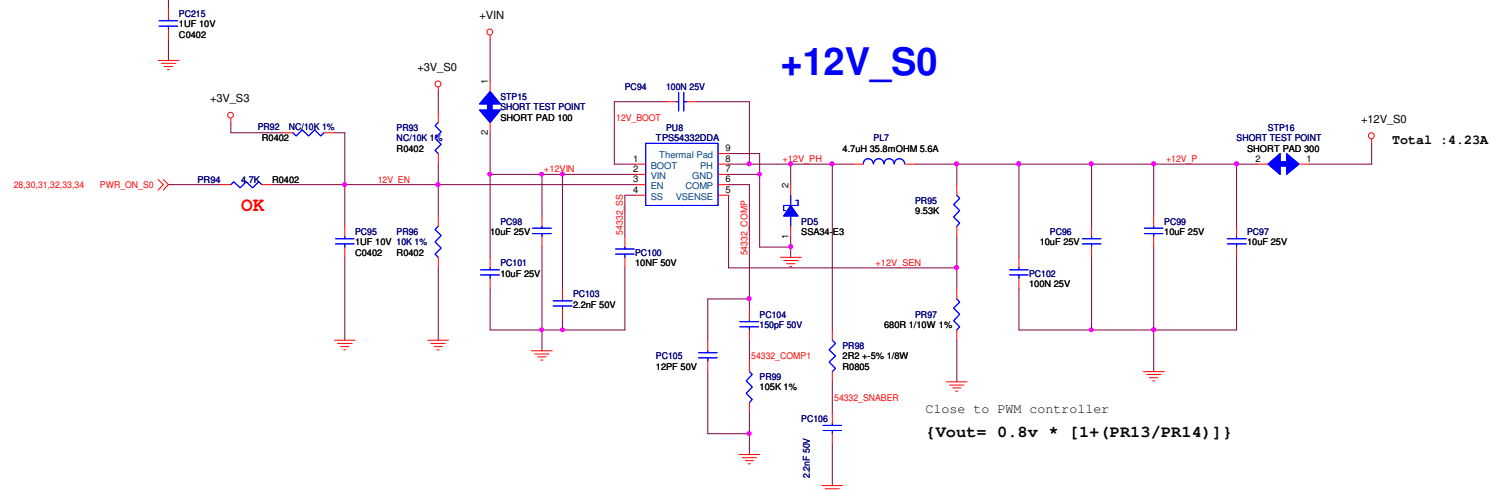


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
Key Component	COVER SHEET	PCB NAME	X000000000000	MOB
Date	Tuesday, May 06, 2012	Sheet	32 of 43	remark

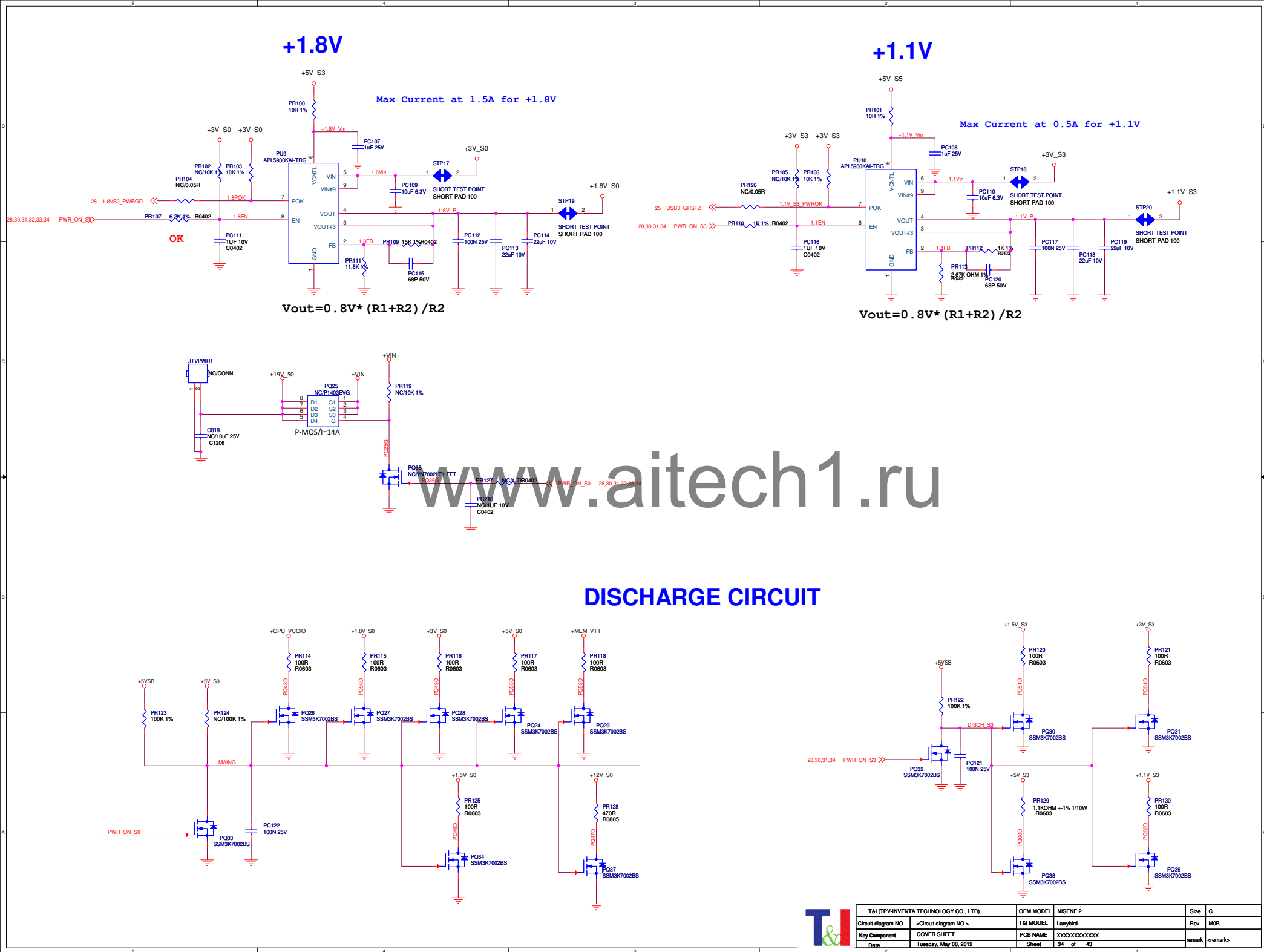
+0.85V



+12V_S0

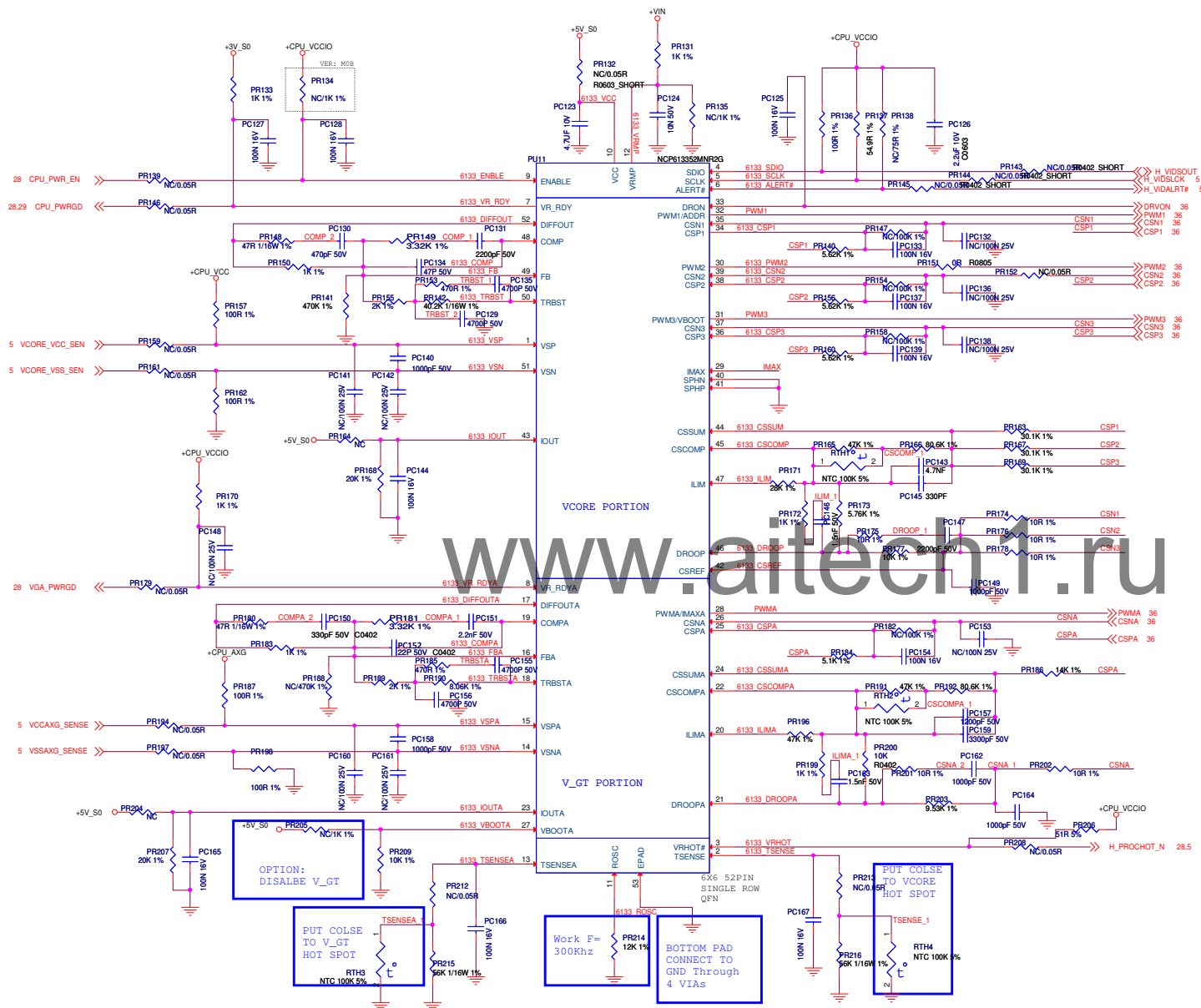


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	Rev
Date	Tuesday, May 06, 2012	Sheet	33 of 43	remark



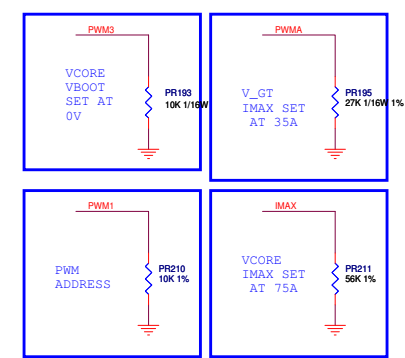
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T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.		T&I MODEL	Lanybird	Rev	M08
COVER SHEET		PCB NAME	XXXXXXXXXXXXXX	remark	
Date		Tuesday, May 06, 2012	Sheet	34 of 43	1

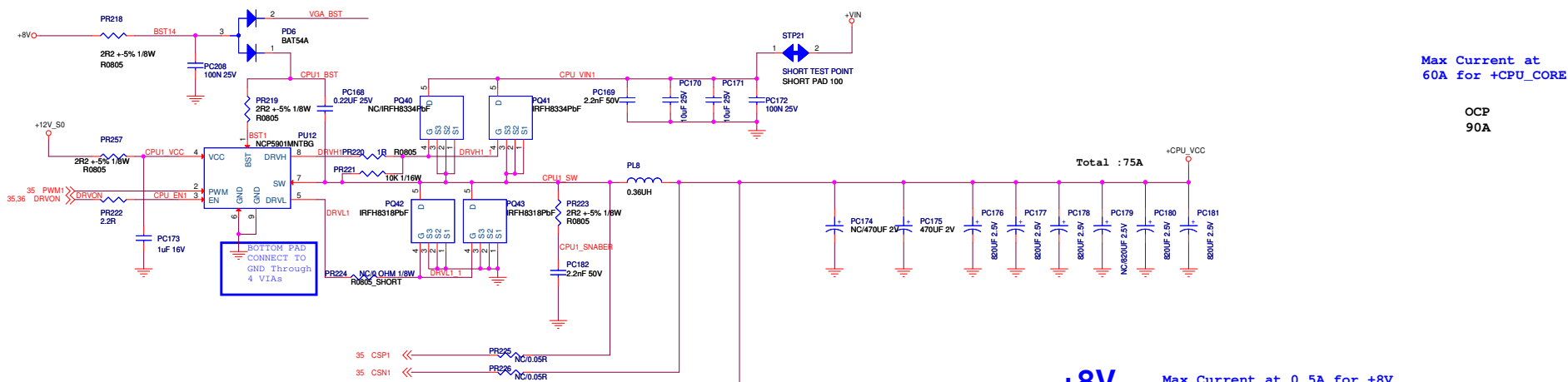


PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR VGT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

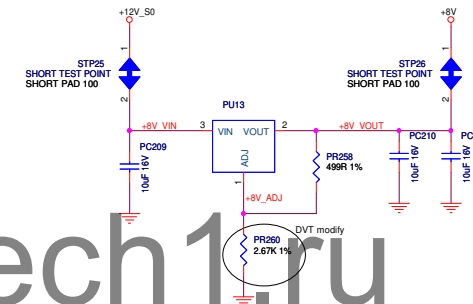
BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V
VCC	SHUTDOWN



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lambird	Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark	<remark>
Date	Tuesday, May 06, 2012	Sheet	35 of 43		

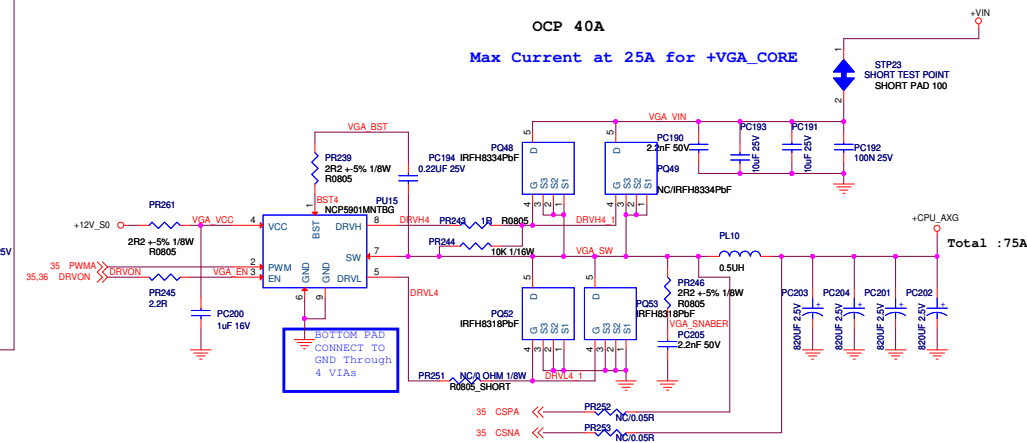


+8V Max Current at 0.5A for +8V



$$VO = VREF \left(1 + \frac{R2}{R1} \right) + IADJ \times R2$$

OCP 40A
Max Current at 25A for +VGA_CORE



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
COVER SHEET		PCB NAME	X00000000000	MOB
Date	Tuesday, May 06, 2012	Sheet	36 of 43	remark

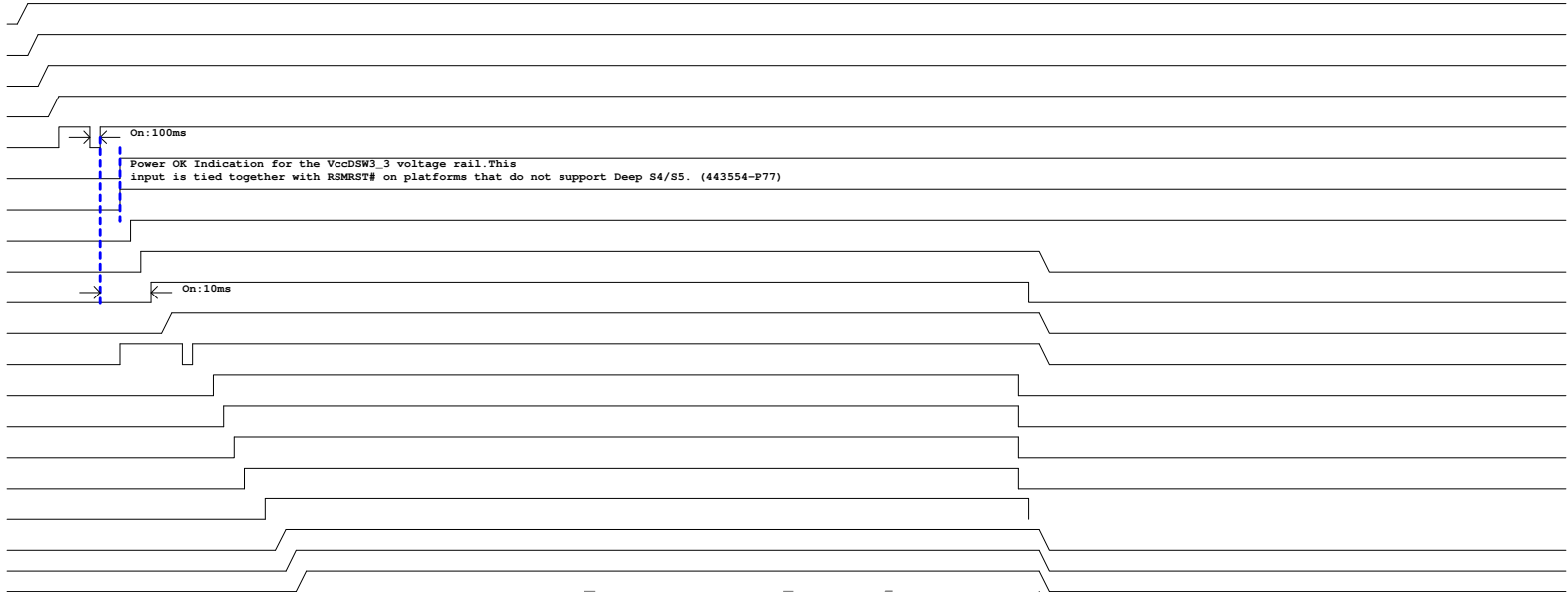
POWER SEQUENCE

Power ON

Power OFF

COIN BATTERY 3V

Net Name	
RTC_BAT	
RTC_RST	
VIN = +19V	
+3VSB/+5VSB	
SYS_PWRBTN#	
PCH_SLP_SUS#	
SUSWARN#&SUSACK#	
PWR_ON_S5	
+3V_S5/+5V_S5	
PCH_RSMRST#	
PCH_DPWRCK	
PCH_PWR_BTN#	
NC_SLP_S5_N	
PCH_SLP_S4#	
PCH_SLP_LAN#>PCH_SLP_A#	
PCH_SLP_S3#	
PWR_ON_S3	
+3v_S3	
+5V_S3	
+1.5V_S3	



S5 PWR

S3 PWR

S0 PWR

KBC OUT	PWR_ON_S0
FOR MXM DESIGN	+5V_S0/+3V_S0
	+MEM_VTT
	+12V_S0
	+1.8V_S0
	+1.5V_S0
	+1.1V_S0
	+1.05V_S0
	+0.85V_S0



CPU PWR

HW_PWRGD	
PCH_APWR_OK	
PCH_PWR_GD	
CPU_PWR_EN	
+CPU_VCC	
+CPU_AXG	
CPU_PWR_GD	
H_DRAMPWRGD	
H_PWRGD	



PCH TO ALL

PLTRST_N	
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T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird	Rev
Key Component	COVER SHEET	PCB NAME	X00000000000X	MOB
Date	Tuesday, May 08, 2012	Sheet	37 of 43	remark
				<remark>

PCH GPIO TABLE

PIN Name	Ball Name	Type	Tolerance	Power Well	Default	Multi Functional	Current Net Name
GPIO0	AW55	I/O	3.3 V	Core	GPI	BMBUSY#	PU_PCH_BMBUSY
GPIO1	BR19	I/O	3.3 V	Core	GPI	TACH1	PU_PCH_GPIO1
GPIO2	BN9	I/OD	5 V	Core	GPI	PIRQE#	PIRQE_N
GPIO3	AV9	I/OD	5 V	Core	GPI	PIRQF#	PIRQF_N
GPIO4	BT15	I/OD	5 V	Core	GPI	PIRQG#	PIRQG_N
GPIO5	BR4	I/OD	5 V	Core	GPI	PIRQH#	PIRQH_N
GPIO6	BA22	I/O	3.3 V	Core	GPI	TACH2	PU_PCH_GPIO6
GPIO7	BR16	I/O	3.3 V	Core	GPI	TACH3	FDO
GPIO8	BP51	I/O	3.3 V	Suspend	GPO	NA	IGC_EN_N
GPIO9	BJ41	I/O	3.3 V	Suspend	Native	OC5#	USB_OC5#
GPIO10	BT45	I/O	3.3 V	Suspend	Native	OC6#	EC_SCI#
GPIO11	BN49	I/O	3.3 V	Suspend	Native	SMBALERT#	SMB_ALERT_N
GPIO12	BK50	I/O	3.3 V	Suspend	Native	LAN_PHY_PWR_CTRL	CLR_BIOS_DATA#
GPIO13	BA25	I/O	3.3 V	Suspend	GPI	HDA_DOCK_RST#	IO_PME_N
GPIO14	BM45	I/O	3.3 V	Suspend	Native	OC7#	EC_SMI#
GPIO15	BM55	I/O	3.3 V	Suspend	GPO	GPIO15	GPIO15
GPIO16	AU56	I/O	3.3 V	Core	GPI	SATA4GP	PCH_GPIO16
GPIO17	BT17	I/O	3.3 V	Core	GPI	TACH0	PCH_EDID_SW
GPIO18	Mobile Only	I/O	3.3 V	Core	Native	NA	NA
GPIO19	AY52	I/O	3.3 V	Core	GPI	SATA1GP	SATA1GP
GPIO20	AV43	I/O	3.3 V	Core	Native	PCIECLKRQ2#	PCIE_LAN_CLKREQ#
GPIO21	BC54	I/O	3.3 V	Core	GPI	SATA0GP	SATA0GP
GPIO22	BA53	I/O	3.3 V	Core	GPI	SCLOCK	PCH_GPIO22
GPIO23	BA20	I/O	3.3 V	Core	Native	LDRQ1#	L_DRQ1_N
GPIO24	BP53	I/O	3.3 V	Suspend	GPO	MEM_LED	H_SKTOCC_N
GPIO25	Mobile Only	I/O	3.3 V	Suspend	Native	NA	NA
GPIO26	Mobile Only	I/O	3.3 V	Suspend	Native	NA	NA
GPIO27	BJ43	I/O	3.3 V	DSW	GPI	GPIO27	PU_PCH_GP27
GPIO28	BJ55	I/O	3.3 V	Suspend	GPO	GPIO28	SLP_LAN_N
GPIO29	BH49	I/O	3.3 V	Suspend	GPI	SLP_LAN#	PCIE_LAN_CLKREQ#
GPIO30	BU46	I/O	3.3 V	Suspend	Native	SUSWARN#	PCH_SUS_WARN#
GPIO31	BG43	I/O	3.3 V	DSW	GPI	GPIO31	PU_PCH_GP31
GPIO32	BC56	I/O	3.3 V	Core	GPO	CLKRUN#	EC_CLKRUN#



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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird		Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX		remark	<remarks>
Date	Tuesday, May 08, 2012	Sheet	38	of	43	

PCH GPIO TABLE

PIN Name	Ball Name	Type	Tolerance	Power Well	Default	Multi Functional	Current Net Name
GPIO33	BC25	I/O	3.3 V	Core	GPO	NA	SOP_ENABLE_GP33
GPIO34	BL56	I/O	3.3 V	Core	GPI	STP_PCI#	PU_PCH_GPIO34
GPIO35	BJ57	I/O	3.3 V	Core	GPO	NMI#	No connected
GPIO36	BB55	I/O	3.3 V	Core	GPI	SATA2GP	PCH_GPIO36
GPIO37	BG53	I/O	3.3 V	Core	GPI	SATA3GP	PCH_GPIO37
GPIO38	BE54	I/O	3.3 V	Core	GPI	SLOAD	BOARD_ID0
GPIO39	BF55	I/O	3.3 V	Core	GPI	SDATAOUT0	REV_ID0
GPIO40	BD41	I/O	3.3 V	Suspend	Native	OC1#	USB_OC1#
GPIO41	BG41	I/O	3.3 V	Suspend	Native	OC2#	USB_OC2#
GPIO42	BK43	I/O	3.3 V	Suspend	Native	OC3#	USB_OC3#
GPIO43	BP43	I/O	3.3 V	Suspend	Native	OC4#	USB_OC4#
GPIO44	BL54	I/O	3.3 V	Suspend	Native	PCIECLKRQ5#	PCIE_WLAN_CLKREQ#
GPIO45	AV44	I/O	3.3 V	Suspend	Native	PCIECLKRQ6#	PCIE_TV_CLKREQ#
GPIO46	BP55	I/O	3.3 V	Suspend	Native	PCIECLKRQ7#	PCIE_USB3_CLKREQ#
GPIO47	Mobile Only	I/O	3.3 V	Suspend	Native	NA	
GPIO48	AW53	I/O	3.3 V	Core	GPI	SDATAOUT1	REV_ID1
GPIO49	BA56	I/O	3.3 V	Core	GPI	SATA5GP	BOARD_ID1
GPIO50	BT5	I/O	5.0 V	Core	Native	REQ1#	REQ1_N
GPIO51	AV8	I/O	3.3 V	Core	Native	GNT1#	GNT1-
GPIO52	BK8	I/O	5.0 V	Core	Native	REQ2#	REQ2_N
GPIO53	BU12	I/O	3.3 V	Core	Native	GNT2#	GNT2-
GPIO54	AV11	I/O	5.0 V	Core	Native	REQ3#	REQ3_N
GPIO55	BE2	I/O	3.3 V	Core	Native	GNT3#	GNT3-
GPIO56	Mobile Only	I/O	3.3 V	Suspend	Native	NA	
GPIO57	BT53	I/O	3.3 V	Suspend	GPI	NA	CLR_PASSWORD#
GPIO58	BJ46	I/O	3.3 V	Suspend	Native	SML1CLK	EC_SCLK0
GPIO59	BM43	I/O	3.3 V	Suspend	Native	OC0#	USB_OC0#
GPIO60	BU49	I/O	3.3 V	Suspend	Native	SML0ALERT#	PCH_GP60_UP
GPIO61	BN54	I/O	3.3 V	Suspend	Native	SUS_STAT#	LPC_PD#
GPIO62	BA47	I/O	3.3 V	Suspend	Native	SUSCLK	BOOT_BLK_REC#
GPIO63	BH50	I/O	3.3 V	Suspend	Native	SLP_S5#	FCH_SLP_S5#
GPIO64	AT9	I/O	3.3 V	Core	Native	CLKOUTFLEX0	No connected
GPIO65	BA5	I/O	3.3 V	Core	Native	CLKOUTFLEX1	Test Point



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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird		Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX		remark	<remarks>
Date	Tuesday, May 06, 2012	Sheet	39 of 43			

PCH GPIO TABLE

PIN Name	Ball Name	Type	Tolerance	Power Well	Default	Multi Functional	Current Net Name
GPIO66	AW5	I/O	3.3 V	Core	Native	CLKOUTFLEX2	Test Point
GPIO67	BA2	I/O	3.3 V	Core	Native	CLKOUTFLEX3	Test Point
GPIO68	BU16	I/O	3.3 V	Core	GPI	TACH4	BOOT_BLK_WR_EN
GPIO69	BM18	I/O	3.3 V	Core	GPI	TACH5	PU_PCH_GPIO69
GPIO70	BN17	I/O	3.3 V	Core	Native	TACH6	PU_PCH_GPIO70
GPIO71	BP15	I/O	3.3 V	Core	Native	TACH7	SCAL_ODD_LED
GPIO72	AV46	I/O	3.3 V	Suspend	Native	BATLOW#	PCH_SPI_WP#_Q
GPIO73	Mobile Only	I/O	3.3 V	Suspend	Native	NA	
GPIO74	BR46	I/O	3.3 V	Suspend	Native	SML1ALERT# or PCHHOT#	PCH_GP74_UP
GPIO75	BK46	I/O	3.3 V	Suspend	Native	SML1DATA	PU_SMLI1DATA

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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird		Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX		remark	<remark>
Date	Tuesday, May 08, 2012	Sheet	42	of	43	

Schematic Modify History

MOA to MOB

Page-5 ,Add C933 C994,Power suggesstion
R687 is change PART ID
Add net "VCC_CPU_+0.85V_SENSE"

Page-9, JDDR1 is change to 10.1mm height
Page-10, JDDR1 is change to 6.0mm height
Page-11, L62,L63 are change PART ID by buyer suggestion
"JLVDS1" reference is change to "UMA_CN1"
"CONVERTER_DPC_TXP0/1" net name are change to "CONVERTER_DPD_TXP0/1"
"CONVERTER_DPC_TXN0/1" net name are change to "CONVERTER_DPD_TXN0/1"
"CONVERTER_DPC_AUXP/N" net name are change to "CONVERTER_DPC_AUXP/N"

Page-12, C810~C817 are not stuff,R798,R799 are not stuff
Net "CPU_GFX_TXP0~15","CPU_GFX_TXN0~15","CPU_GFX_RXP0~15" and "CPU_GFX_RXN0~15"
seriacl CAP are change to 0.22uF
Stuff R802,un-stuff R805 for Nvidia suggestion

Page-13,R838 is stuff,R1143 un-stuff for EC & BIOS suggestion
Add R1144,C991 for power soft star
Add net "EC_SCLK0","EC_SDATA0" for EDID flash issue

Page-14,Net "PCIE_TV_RXN/P" and "PCIE_TV_TXN/P" are change connect to PCH PCIE port5
Net "PCIE_WLAN_RXN/P" and "PCIE_WLAN_TXN/P" are change connect to PCH PCIE port6
Net "USB_OC6#" rename to EC_SCI# for BIOS suggestion

Page-15,R935 is change to 1K ohm,R331 is change to 0 ohm,R936 is change to 4.7k ohm follow Intel CRB
R951 and R952 are stuff 10k ohm to disable DDPB,DDPC
Net "PCH_DVI_DATA0~2P/N" are change to DDPC,Net "CONVERTER_DPDTX0~1P/N" are change to DDPD
ODD change to connect Net "SATA_RX4N/P" and "SATA_TX4N/P"
R940 and R941 are stuff 10k ohm,R946 and R947 are stuff 10k ohm

Page-16,X5 is changed PART ID by buyer suggestion
R1123 and R1020 are un-stuff,add R1121 for PCH clear CMOS
Add JME1 for BIOS request,add R1122 follow Intel CRB

Page-17,L59 is changed PART ID by buyer suggestion
Page-18,R1069 and R1070 are un-stuff for BIOS & EC suggestion
Page-19,R934 is un-stuff for can't boot issue
Page-20,JMIC1 is change PART ID by buyer suggestion
Page-21,JHP1 and JLINEOUT1 change PART ID by buyer suggestion
Page-22,Remove Q50 for can't boot issue
Add 0ohm R1127,R373 is change to 2.2k ohm,Q32 is unstuff
Page-22,Remove Q50 for can't boot issue
Add 0ohm R1127,R373 is change to 2.2k ohm,Q32 is unstuff for 100mW issue

Page-23,JCR1 is change PART ID
JSATAHDD1 is change white color,JSATAODD1 is change blue color

Page-24,R384,R386,R392,R385,R389,R395,R579,R580 and R571 are change to 0805 footprint
Add 0ohm R621 reset signal for 80 port

Page-25,C921 and C922 are change 18pF for SI pass

Page-26,JUSB30L1,JUSB30L2,JUSBR0~3 and JUSBDON1 are change PART ID for ME height request

Page-27,Add R1141,R1142 for S3 wake
Add manual parts PCB1,CPU_BACK1,CPU_STAIN1,CPU HOLDER1,JECSP12,JFCHSPI2,JUMP1~3 and JRTCBATT2

Page-28,U36 is change G781-1P8F,remove U28,Q41 for address conflick issue
R471 is un-stuff; R506,R507 are change connect to +3V_S5
R466,R467 are change to 10k ohm for <100mW issue

Page-29,Remove R332,R333,R334,R338,R342,R575,R576 and R577
Page-30,PR5,PR6 are change PART ID for power suggestion
PR19 is stuff,PR21 is un-stuff for AUDIO headphone in S3 noisy issue
Reserve PC213 for power suggestion

Page-31,PR41 is change PART ID for power suggestion
PC46, PR49, PU3, PR48 and PC47 are un-stuff for < 100mW issue

Page-32,PR60 and PR71 are change connect to +3V_S0
PR66 and PR77 are change PART ID for power suggestion
PQ56 is change use BJT for vlotage select issue

Page-33,PR82 is change connect to +3V_S0 ; PR88 PART ID is change,Add PR274 for CPU voltage sense
PQ58 is change use BJT for vlotage select issue

Page-35,PR134 is un-stuff for power sequence issue

Page-36,PR260 is change PART ID for power suggestion

PVT & MP de-pop circuit

page 16 for EC debug connector
JECDB1

page 17 for HP debug
JLPCDB1,R310,JHPDB5,C147,U31,Q22,D9~D14,R312~R317

page 17 for AMD debug
U5,R53,R56,R77,R80

page 17 for TnI HW debug (CRT output function)
C3,C4,C7,C14,C15,C16,C21,C22,D22,D23,JCRTDB1
L1,L2,L3,Q1,Q2,R1,R2,R3,R4,R5,R6,R10,R11,R14
R15,R25,R26,R28,R29,R30,R32,R36,R37,U1,U2

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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Lanybird		Rev	MOB
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX		remark	<remark>
Date	Tuesday, May 06, 2012	Sheet	43	of	43	